

## DATA SHEET

### NV3051F1

2400-channel 8-bit Source Driver and GOA/GIP Gate Driver with System-on chip for Color Amorphous TFT-LCDs

Version 0.3  
Dec. 2020

## Contents

1. Introduction .....	4
2. Features.....	5
3. Block Diagram.....	7
3.1 Block Function:.....	7
3.1.1 System interface .....	8
3.1.2 Grayscale voltage generating circuit .....	8
3.1.3 Timing controller .....	8
3.1.4 Oscillator (OSC).....	8
3.1.5 Source driver circuit.....	8
3.1.6 Gate driver circuit .....	8
3.1.7 LCD driving power supply circuit.....	8
4. PIN DESCRIPTIONS .....	9
4.1 Pin Definition.....	9
4.2. Power Block Diagram.....	15
4.3. Power Supply Configuration.....	16
4.3.1. Mode 3: Power IC mode (Mode-3 BOOSTM=2'b10) .....	17
4.3.2. Mode 8: External VSP and VSN (Mode-8 BOOSTM=2'b01).....	18
4.4 BOM List .....	19
4.4.1. Mode-3: Power IC mode.....	19
4.4.2. Mode-8: External VSP and VSN .....	19
5. INSTRUCTIONS .....	20
5.1. Outline.....	20
5.2. SYSTEM COMMAND DESCRIPTION .....	24
5.2.1. NOP (00h).....	24
5.2.2. Software Reset(01h).....	25
5.2.3 Read Display ID(04h).....	26
5.2.4. Read Display Power Mode(0Ah).....	27
5.2.5. Read Display MADCTL(0BH).....	28
5.2.6. Read Display Pixel Format(0CH).....	29
5.2.7. Read Display Image Mode(0DH).....	30
5.2.8. Read Display Signal Mode(0EH) .....	31
5.2.9. Read Display Self-Diagnostic Result(0FH).....	32
5.2.10. Sleep In(10h).....	33
5.2.11. Sleep Out(11H).....	34
5.2.12. Normal Display Mode On(13H) .....	35
5.2.13. Display Inversion Off(20H).....	36
5.2.14. Display Inversion On(21H).....	37
5.2.15. All Pixel Off(22H) .....	38
5.2.16. All Pixels On(23H).....	39
5.2.17. Display Off(28H).....	40
5.2.18. Display On(29H).....	41
5.2.19. Tearing Effect Line OFF(34H).....	42
5.2.20. Tearing Effect Line ON(35H).....	43

5.2.21. Display Access Control(36H).....	44
5.2.22. Idle Mode Off(38H).....	45
5.2.23. Idle mode on and other mode off (39H) .....	46
5.2.24. Write Tear Scan Line(44H) .....	47
5.2.25. Read Scan Line(45H).....	48
5.2.26. Write Tear Scan Line Width(46H) .....	49
5.2.27. Read Tear Scan Line Width(47H) .....	50
5.2.28. Write Display Brightness Value(51H).....	51
5.2.29. Read Display Brightness Value(52h).....	52
5.2.30. Write CTRL Display Value(53H).....	53
5.2.31. Read CTRL Display Value(54H).....	54
5.2.32. Read Display ID1(DAH) .....	55
5.2.33. Read Display ID2(DBH).....	56
5.2.34. Read Display ID3(DCH).....	57
5.2.35. EXTC Command Set enable register (FFH).....	58
5.3. Customer Command List and Description.....	61
5.3.1. IFCTRL2:21H.....	61
5.3.2. vcom_adj:37H~3AH.....	62
5.3.3. PADCTRL1: 48H .....	67
5.3.4. BOOST_CTRL1~2 : 80h~81h.....	68
5.3.5. EXTPW_CTRL1~3:90H~92H .....	69
5.3.6. PUMP_CTRL1~4:98H~9BH.....	71
5.3.7.LVDS_CTRL0,LVDS_CTRL8:D0H,D7H.....	75
5.3.8. ENEXTC:FFH .....	76
5.3.9. PGAMVR0~5;PGAMPR0~1;PGAMPK0~9;GAMP0:B0H~C2H.....	80
5.3.10. NGAMVR0~5;NGAMPR0~1;NGAMPK0~9;GAMN0:D0H~E2H.....	81
5.3.11. ENEXTC:FFH .....	82
<b>6. FUNCTIONS.....</b>	<b>83</b>
6.1. Interface Type Selection .....	83
6.2. MIPI-DSI Interface .....	84
6.2.1. General description .....	84
6.2.2. Interface level communication.....	84
6.2.2.1. General.....	84
6.2.2.2. DSI-CLK lanes.....	86
6.2.3. DSI data lanes .....	92
6.2.3.1. General.....	92
6.2.3.2. Escape modes.....	92
6.2.3.3. High-Speed Data Transmission (HSDT) .....	98
6.2.3.4. Bus Turnaround (BTA).....	100
6.2.3.5. Two Data-lane High Speed Transmission .....	101
6.2.3.6. Three data-lane high speed transmission .....	102
6.2.4. Packet level communication .....	103
6.2.4.1. Short Packet (Spa) and Long Packet (Lpa) structures .....	103
6.2.4.2. Packet transmissions .....	112
6.2.5. Customer-defined generic read data type format.....	115

6.2.6. MIPI video parameter .....	116
6.3. Serial Interface (SPI).....	120
6.3.1. SPI write mode.....	120
6.3.2. SPI read mode .....	120
6.4. LVDS interface .....	121
6.4.1 Data input format for LVDS .....	121
6.5. Sleep Out-Command And Self-Diagnostic Functions Of The Display Module.....	123
6.5.1. Register loading detection.....	123
6.5.2. Functionality detection.....	124
6.6. Power On/Off Sequence .....	125
6.6.1. Case 1 – RESX line is held high or unstable by host at power on.....	126
6.6.2. Case 2 – RESX line is held low or unstable by host at power on.....	127
6.6.3. Uncontrolled power off.....	127
<b>7. ELECTRICAL SPECIFICATION .....</b>	<b>128</b>
7.1. Absolute Maximum Ratings .....	128
7.2. DC characteristic.....	129
7.2.1. Basic DC characteristic.....	129
7.2.2. MIPI DC character.....	131
7.3. AC characteristic.....	133
7.3.1. Reset timing characteristics .....	133
7.3.2. Serial interface characteristics (SPI).....	134
7.3.3. MIPI-DSI characteristics .....	136
7.3.3.1. High speed mode.....	136
7.3.3.2. Low power mode .....	138
7.3.3.3. Bursts .....	139
7.3.4 LVDS AC characteristic .....	141
<b>8. CHIP INFORMATION .....</b>	<b>143</b>
8.1. PAD Assignment .....	143
8.2. Alignment Mark.....	145
<b>9. DISCLAIMER.....</b>	<b>146</b>
Revision history.....	147

## **1.Introduction**

The NV3051F1, a 16,777,216-color System-on-Chip (SoC) RAMless driver LSI designed for small and medium size TFT LCD display, is capable of supporting up to 800xRGBx2048 pixels in resolution. The 2400-channel source driver can provide true 8-bit resolution and generate 256 Gamma-corrected values with an internal D/A converter.

The NV3051F1 is able to operate with low IO interface power supply. Incorporating with several charge pumps, the NV3051F1 can generate various voltage levels by an on-chip power management system for gate and source driver.

The built-in timing controller in the NV3051F1 can support several functions to meet a wide variety of requirements about portable display applications. It provides several system interfaces, including MIPI/SPI/LVDS, which can be used to configure the system. Furthermore, it can also achieve high speed display data transmission by using the MIPI video mode.

The NV3051F1 also provides standby mode for power control considerations. For further power control requirements, the dynamic backlight control function, which is based on the image content, is also supported.

## 2. Features

- ◎ **One-chip solution for color amorphous TFT-LCD and IGZO-LCD**
- ◎ **Display Resolution**
  - 800 x RGB x (1280, others), (Source output from S1 to S1200, S1201 to S2400)
  - 768 x RGB x (1280, others), (Source output from S1 to S1152, S1249 to S2400)
  - 750 x RGB x (1334, others), (Source output from S55 to S1152, S1249 to S2400)
  - 750 x RGB x (1334, others), (Source output from S1 to S1152, S1249 to S2346)
  - 750 x RGB x (1334, others), (Source output from S1 to S1125, S1276 to S2400)
  - 720 x RGB x (1280, others), (Source output from S1 to S1080, S1321 to S2400)
  - 640 x RGB x (1280, others), (Source output from S1 to S960, S1441 to S2400)
  - 600 x RGB x (1280,1024, others), (Source output from S1 to S900, S1501 to S2400)
  - 540 x RGB x (1280,960, others), (Source output from S1 to S810, S1591 to S2400)
  - 480 x RGB x (1280,960, others), (Source output from S1 to S720, S1681 to S2400)
  - 480 x RGB x (1280,960, others), (Source output from S961 to S1200, S1201 to S2400)
  - 480 x RGB x (1280,960, others), (Source output from S1 to S900, S1501 to S2040)
  - 400 x RGB x (1280,960, others), (Source output from S1201 to S2400)
  - 400 x RGB x (1280,960, others), (Source output from S1 to S600, S1801 to S2400)
  - 320 x RGB x (1280,960, others), (Source output from S1441 to S2400)
- ◎ **Display Data Memory: None (RAMless)**
- ◎ **System Interfaces**
  - MIPI DSI (2/3/4 data lane): MIPI DSI (DSI v1.01.00, D-PHY v1.00.00 and DCS v1.01).
  - SPI interface
  - LVDS interface
- ◎ **Display Features**
  - Outputs 256 $\gamma$ -corrected values and using an internal true 8-bit resolution D/A converter to achieve 16,777,216 colors
- ◎ **Display Modes**
  - Power saving mode (standby)
  - Low power consumption structure for source driver
- ◎ **On Chip Function**
  - Support DC-VCOM driving scheme
  - RAMless driver with MIPI video mode
  - RAMless driver with LVDS video mode
  - Built-in internal oscillator and hardware reset

- On-chip OTP program voltage generator
- Built-in OTP (3 Times) to store ID1~ID3
- Built-in OTP (2 Times) to store gamma curve
- Built-in OTP (1 Time) to store VGMP, VGMN, VCOM calibration
- Built-in 3 power structure modes for application
- Source output voltage level VGMP-AGND: 2.64 ~ 5.85V , VGMN-AGND: -2.51 ~ -5.70V

◎ **Power Supply Range**

- External power IC:

- I/O pads supply voltage (IOVCC): 1.65 ~ 3.6V
- Power supply for MIPI regulator circuit (VDDAM): 1.75 ~ 3.6V
- Analog power supply voltage (VCI): 2.5 ~ 3.6V

- Three-Power Mode:

- I/O pads supply voltage (IOVCC): 1.65 ~ 3.6V
- Power supply for MIPI regulator circuit (VDDAM): 1.75 ~ 6V
- Analog power supply (VSP) : 4.5V to 6V
- Analog power supply (VSN) : -4.5V to -6V

Note:  $3V \leq IOVCC \leq 3.6V$  for using LVDS.





### **3.1.1 System interface**

The NV3051F1 supports the video data transmitted through the high-speed system interface, MIPI (Mobile Industry Processor Interface) and LVDS.

### **3.1.2 Grayscale voltage generating circuit**

NV3051F1 has true 8-bit resolution D/A converter, which generates 256 Gamma-corrected values and cooperates with OP-AMP structure to enhance display quality. The grayscale voltage can be adjusted by grayscale data set in the  $\gamma$ -correction register.

### **3.1.3 Timing controller**

NV3051F1 has a timing controller, which can generate a timing signal for internal circuit operation such as gate output timing, image data accessing timing, etc.

### **3.1.4 Oscillator (OSC)**

The NV3051F1 also features an internal oscillator. In standby mode, the oscillator is halted to reduce power consumption.

### **3.1.5 Source driver circuit**

NV3051F1 consists of a 2400-output source driver circuit (S1 to S1200, S1201 to S2400) and several source dummy outputs (SDUM3; SDUM0; S[2401]; S[0]). Data transmitted through MIPI video mode are latched when a single line data has been accumulated. And then the latched data controls the source driver and generates a drive waveform.

### **3.1.6 Gate driver circuit**

NV3051F1 consists of output gate driver control circuit. The gate driver circuit outputs gate driver signals at either VGH or VGL level.

### **3.1.7 LCD driving power supply circuit**

The LCD driving power supply circuit generates the voltage levels VGH, VGL and VCOM for driving an LCD. All these voltages can be adjusted by register setting.

## 4. PIN DESCRIPTIONS

### 4.1 Pin Definition

Signal	I/O	PAD Type (Voltage Level)	Function
<b>Global Control Signal</b>			
RS[1]	I	Digital Input (IOVCC-VSSI)	When rising edge,turn on the chip and enter the display on mode.If no used,let it open.
RESX	I	Digital Input (IOVCC-VSSI)	Global Reset Signal. Active Low.
TE	O	Digital Output (IOVCC-VSSI)	Tearing effect output pin is used to synchronize MCU frame writing, activated by S/W command. When this pin is not activated (TE function OFF), this pin is VSSI level.
TE1	O	Digital Output (IOVCC-VSSI)	Output pin for scan line signal, activated by S/W command. When this pin is not activated, this pin is VSSI level.
LEDPWM	O	Digital Output (IOVCC-VSSI)	LCD backlight control PWM output pin.
PWM_VSN	O	Digital Output (VSSI-VSN)	LCD backlight control PWM output pin.
LED_K1~ LED_K5	O	-	LCD backlight control on chip switch drain output.(3V backlight)

MIPI Interface																																																																																			
IM[2:0]	I	Digital Input (IOVCC-VSSI)	<p>Interface mode select pins.IM [2]: Internal pull low.</p> <p>Notes:</p> <p>(1) IM[2:0] pins are used to configure lane sequence and polarity.</p> <p>(2) The bottom table is an example for MIPI 4 lane setting.</p> <table border="1"> <thead> <tr> <th colspan="3">External Pad Set</th> <th colspan="5">Configuration of MIPI Lane</th> </tr> <tr> <th>IM[2]</th> <th>IM[1]</th> <th>IM[0]</th> <th>D0P/N</th> <th>D1P/N</th> <th>CLKP/N</th> <th>D2P/N</th> <th>D3P/N</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>D3P/N</td> <td>D2P/N</td> <td>CLKP/N</td> <td>D1P/N</td> <td>D0P/N</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>D3N/P</td> <td>D2N/P</td> <td>CLKN/P</td> <td>D1N/P</td> <td>D0N/P</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>D0P/N</td> <td>D1P/N</td> <td>CLKP/N</td> <td>D2P/N</td> <td>D3P/N</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>D0N/P</td> <td>D1N/P</td> <td>CLKN/P</td> <td>D2N/P</td> <td>D3N/P</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>D3P/N</td> <td>D0P/N</td> <td>CLKP/N</td> <td>D1P/N</td> <td>D2P/N</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>D3N/P</td> <td>D0N/P</td> <td>CLKN/P</td> <td>D1N/P</td> <td>D2N/P</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>D2P/N</td> <td>D1P/N</td> <td>CLKP/N</td> <td>D0P/N</td> <td>D3P/N</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>D2N/P</td> <td>D1N/P</td> <td>CLKN/P</td> <td>D0N/P</td> <td>D3N/P</td> </tr> </tbody> </table>	External Pad Set			Configuration of MIPI Lane					IM[2]	IM[1]	IM[0]	D0P/N	D1P/N	CLKP/N	D2P/N	D3P/N	0	0	0	D3P/N	D2P/N	CLKP/N	D1P/N	D0P/N	0	0	1	D3N/P	D2N/P	CLKN/P	D1N/P	D0N/P	0	1	0	D0P/N	D1P/N	CLKP/N	D2P/N	D3P/N	0	1	1	D0N/P	D1N/P	CLKN/P	D2N/P	D3N/P	1	0	0	D3P/N	D0P/N	CLKP/N	D1P/N	D2P/N	1	0	1	D3N/P	D0N/P	CLKN/P	D1N/P	D2N/P	1	1	0	D2P/N	D1P/N	CLKP/N	D0P/N	D3P/N	1	1	1	D2N/P	D1N/P	CLKN/P	D0N/P	D3N/P
External Pad Set			Configuration of MIPI Lane																																																																																
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0	0	0	D3P/N	D2P/N	CLKP/N	D1P/N	D0P/N																																																																												
0	0	1	D3N/P	D2N/P	CLKN/P	D1N/P	D0N/P																																																																												
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1	1	1	D2N/P	D1N/P	CLKN/P	D0N/P	D3N/P																																																																												
LANSEL	I	Digital Input (IOVCC-VSSI)	<p>MIPI DSI Lane number selection pin.</p> <p>LANSEL="1", MIPI DSI is 2 Lane mode.</p> <p>LANSEL="0", MIPI DSI is 3 or 4 Lane mode.</p>																																																																																
CLKP	I	MIPI Input (MV1P2-MGND)	MIPI-DSI clock Lane positive-end input pin.																																																																																
CLKN	I	MIPI Input (MV1P2-MGND)	MIPI-DSI clock Lane negative-end input pin.																																																																																
D0P	I/O	MIPI I/O (MV1P2-MGND)	MIPI-DSI data Lane 0 positive-end input/output pin. Please connected to MGND if not used.																																																																																
D0N	I/O	MIPI I/O (MV1P2-MGND)	MIPI-DSI data Lane 0 negative-end input/output pin. Please connected to MGND if not used.																																																																																
D1P	I/O	MIPI I/O (MV1P2-MGND)	MIPI-DSI data Lane 1 positive-end input/output pin. Please connected to MGND if not used.																																																																																
D1N	I/O	MIPI I/O (MV1P2-MGND)	MIPI-DSI data Lane 1 negative-end input/output pin. Please connected to MGND if not used.																																																																																
D2P	I/O	MIPI I/O (MV1P2-MGND)	MIPI-DSI data Lane 2 positive-end input/output pin. Please connected to MGND if not used.																																																																																
D2N	I/O	MIPI I/O (MV1P2-MGND)	MIPI-DSI data Lane 2 negative-end input/output pin. Please connected to MGND if not used.																																																																																
D3P	I/O	MIPI I/O (MV1P2-MGND)	MIPI-DSI data Lane 3 positive-end input/output pin. Please connected to MGND if not used.																																																																																
D3N	I/O	MIPI I/O (MV1P2-MGND)	MIPI-DSI data Lane 3 negative-end input/output pin. Please connected to MGND if not used.																																																																																

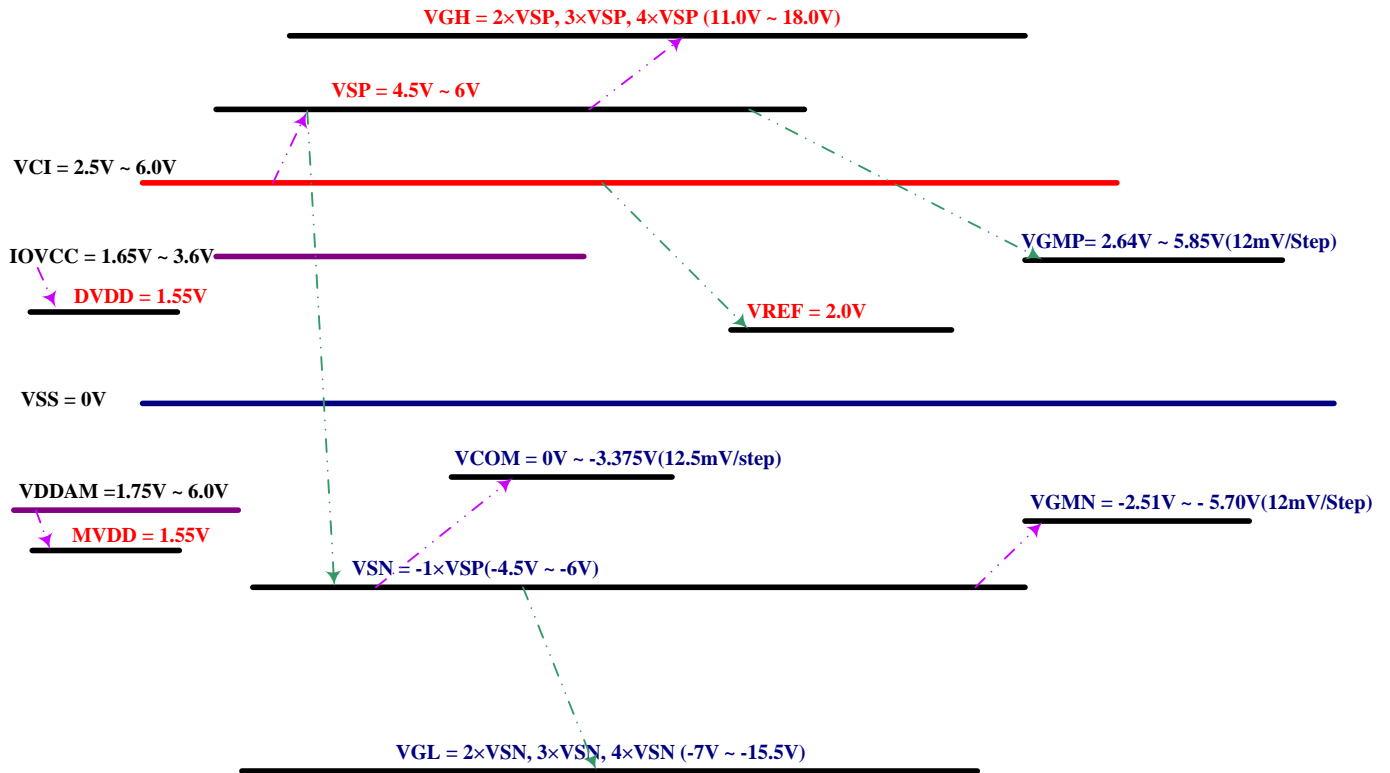
LVDS Interface																													
LVDS_CKP/N	I	LVDS input (IOVCC-VSSI)	LVDS clock Input.																										
LVDS_D0P/N~LVDS_D3P/N	I	LVDS input (IOVCC-VSSI)	LVDS data Input.																										
SPI Interface																													
CSX	I	Digital Input (IOVCC-VSSI)	Chip select signal for SPI interface operation. ”0” : the NV3051F1 is accessible. ”1” : the NV3051F1 is not accessible. If not used, please fix to the IOVCC or VSSI.																										
SCL	I	Digital Input (IOVCC-VSSI)	SCL: Serial interface Clock Input. If not used, please fix to the IOVCC or VSSI.																										
SDI	I/O	Digital I/O (IOVCC-VSSI)	SDI: Serial interface DATA Input/Output. If not used, please fix to the IOVCC or VSSI.																										
SDO	O	Digital Output (IOVCC-VSSI)	Serial interface DATA output. If not used, please let it open.																										
Source Control Signals																													
S[2400:0]	O	Analog Output (VSP-VSN)	Output source driver signals. The D/A converted 256-gray-scale analog voltage is output. Source output mapping with different resolution. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Resolution</th> <th>Source channel</th> </tr> </thead> <tbody> <tr> <td>800RGB</td> <td>S[2400:1201],S[1200:1]</td> </tr> <tr> <td>768RGB</td> <td>S[2400:1249],S[1152:1]</td> </tr> <tr> <td rowspan="3">750RGB</td> <td>S[2400:1249],S[1152:55]</td> </tr> <tr> <td>S[2346:1249],S[1152:1]</td> </tr> <tr> <td>S[2400:1276],S[1125:1]</td> </tr> <tr> <td>720RGB</td> <td>S[2400:1321],S[1080:1]</td> </tr> <tr> <td>640RGB</td> <td>S[2400:1441],S[960:1]</td> </tr> <tr> <td>600RGB</td> <td>S[2400:1501],S[900:1]</td> </tr> <tr> <td>540RGB</td> <td>S[2400:1591],S[810:1]</td> </tr> <tr> <td rowspan="2">480RGB</td> <td>S[2400:1681],S[720:1]</td> </tr> <tr> <td>S[2400:1201],S[1200:961]</td> </tr> <tr> <td rowspan="2">400RGB</td> <td>S[2400:1201]</td> </tr> <tr> <td>S[2400:1801],S[600:1]</td> </tr> <tr> <td>320RGB</td> <td>S[2400:1441]</td> </tr> </tbody> </table>	Resolution	Source channel	800RGB	S[2400:1201],S[1200:1]	768RGB	S[2400:1249],S[1152:1]	750RGB	S[2400:1249],S[1152:55]	S[2346:1249],S[1152:1]	S[2400:1276],S[1125:1]	720RGB	S[2400:1321],S[1080:1]	640RGB	S[2400:1441],S[960:1]	600RGB	S[2400:1501],S[900:1]	540RGB	S[2400:1591],S[810:1]	480RGB	S[2400:1681],S[720:1]	S[2400:1201],S[1200:961]	400RGB	S[2400:1201]	S[2400:1801],S[600:1]	320RGB	S[2400:1441]
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	S[2400:1801],S[600:1]																												
320RGB	S[2400:1441]																												
SDUM[3] S[2401]	O	Analog Output (VSP-VSN)	Source dummy output.																										
S[0] SDUM[0]	O	Analog Output (VSP-VSN)	Source dummy output.																										

Panel Control and VCOM Pins			
GOUTL [22:1]	O	Analog Output	Gate control signals for panel in left side of IC.
GOUTR [22:1]	O	Analog Output	Gate control signals for panel in right side of IC.
VCOM_L	O	DUMMY Pin	VCOM DUMMY Pin.
VCOM_R	O	Analog Output	VCOM signal output.
VCOM_DUM	O	DUMMY Pin	VCOM DUMMY Pin.
Charge Pump / Boost			
VSP	I	Analog Input	Input voltage from the set-up circuit (4.5V to 6V).
VSN	I	Analog Input	Input voltage from the set-up circuit (-4.5V to -6V).
VGH	O	Analog Output	Positive Power Supply for Gate Driver. VGH=2xVSP, 3xVSP, 4xVSP
VGL	O	Analog Output	Negative Power Supply for Gate Driver. VGL=2xVSN, 3xVSN, 4xVSN
VGH1	O	Analog Output	This pin is used to discharge function. Connect to a capacitor between VGH1 and system ground. If not used, please let this pin short to VGH.
VGH2	O	Analog Output	This pin is used to discharge function. Connect to a capacitor between VGH2 and system ground. If not used, please let this pin short to VGH.
DCHR1	O	Resister	External discharge for VGH1 voltage. Connect to a resister between DCHR1 and system ground.
DCHR2	O	Resister	External discharge for VGH2 voltage. Connect to a resister between DCHR2 and system ground.
EXTP	O	Analog Output	Booster/charge pump power IC output to generate VSP.
EXTN	O	Analog Output	Booster/charge pump power IC output to generate VSN.
Regulator Relative Pins			
VGMP	O	Analog Output	Output voltage generated from VSP. It's used for positive gray scale voltage.
VGMN	O	Analog Output	Output voltage generated from VSN. It's used for negative gray scale voltage.
VREF	O	Analog Output	Reference Voltage for internal voltage generating circuits.

<b>Power Supply and Regulator pins</b>			
VCI	I	Power Supply	Power supply for analog circuits. (VCI=2.5V to 6V)
VDDAM	I	Power Supply	Power Supply for MIPI regulator circuits.(VDDAM=1.75V to 6V)
IOVCC	I	Power Supply	External Power Supply for IO pads and other logic circuits. (IOVCC=1.65 to 3.6V)
VPP	I	Power Supply	Input power for NV memory programming. Input power range: 8.0V ~ 8.5V (Typical=8.25V). When not under programming, VPP pin can be float or tied to ground.
AGND	I	Ground	Analog Ground for analog circuits.
VSSI	I	Ground	I/O Ground for I/O logic circuits.
VSSI_LVDS	I	Ground	I/O Ground for LVDS logic circuits.
DGND	I	Ground	Digital Ground for digital circuits.
DGND_LVDS	I	Ground	Digital Ground for LVDS circuits.
MGND	I	Ground	MIPI Ground for MIPI circuits.
RGND	I	Ground	Analog Ground for regulators.
CGND1	I	Ground	Analog Ground for PUMP's.
DVDD	O	Analog Output	Internal Power Supply for Digital Logic Circuits.
DVDD_LVDS	O	Analog Output	Internal Power Supply for LVDS Logic Circuits.
MVDD	O	Analog Output	Internal Power Supply for MIPI.

Test/Dummy Signal			
TEST_EN	I	Digital Input (IOVCC-VSSI)	Internal pull low, digital test enable, active high. If not used, please let it open or connect to VSSI.
BIST_EN	I	Digital Input (IOVCC-VSSI)	Internal pull low, CP test enable, active high. If not used, please let it open or connect to VSSI.
CLK_SEL	I	Digital Input (IOVCC-VSSI)	Test pin, internal pull low. If not used, please let it open or connect to VSSI.
EXT_CLK	I	Digital Input (IOVCC-VSSI)	Test pin, If not used, please let it open or connect to VSSI.
TEST[3:0]	I	Digital Input (IOVCC-VSSI)	Test pins. Please let them float or connect to VSSI.
TOUT[3:0]	O	Digital Output (IOVCC-VSSI)	Test output pins. Please let them float.
DUMMYR1;DUMMYR2	-	-	Dummy pins. For bonding resistance measurement. There are two pads here, propose to connect them separately.
DUMMY	-	-	Bottom of the chip. Dummy pins. They are not used, left it open.
DUMMY3- DUMMY30/DUMMY151 - DUMMY174/ DUMMY295- DUMMY322	-	-	Top of the chip. Dummy pins. They are not used, left it open.
NC	-	-	Not connect.

## 4.2. Power Block Diagram





### 4.3. Power Supply Configuration

Two power structures for different applications controlled by BOOSTM[1:0](register control),like the following table.

<b>BOOSTM1</b>	<b>BOOSTM0</b>	<b>Mode</b>
0	1	Mode-8, External VSP and VSN
1	0	Mode-3, Power IC

These pins must connect to VSSI or IOVCC level.

4.3.1. Mode 3: Power IC mode (Mode-3 BOOSTM=2'b10)

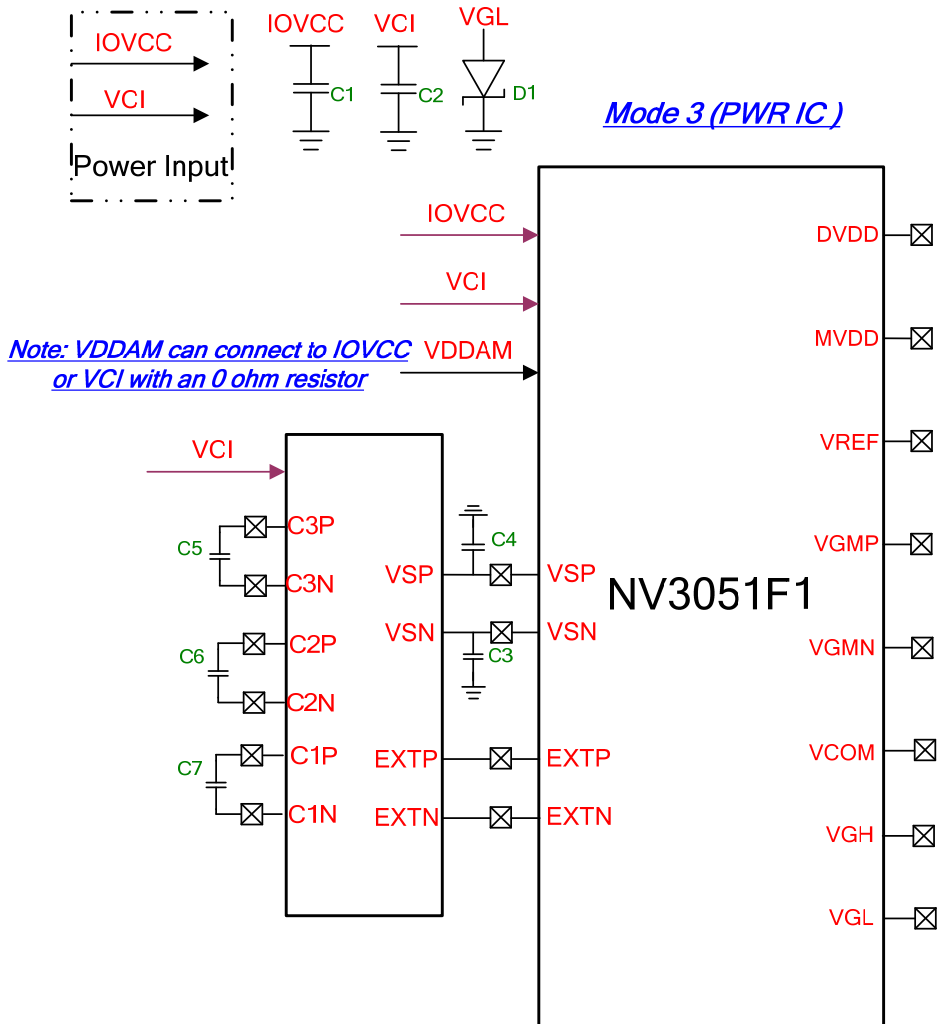


Fig 4.1

4.3.2. Mode 8: External VSP and VSN (Mode-8 BOOSTM=2'b01)

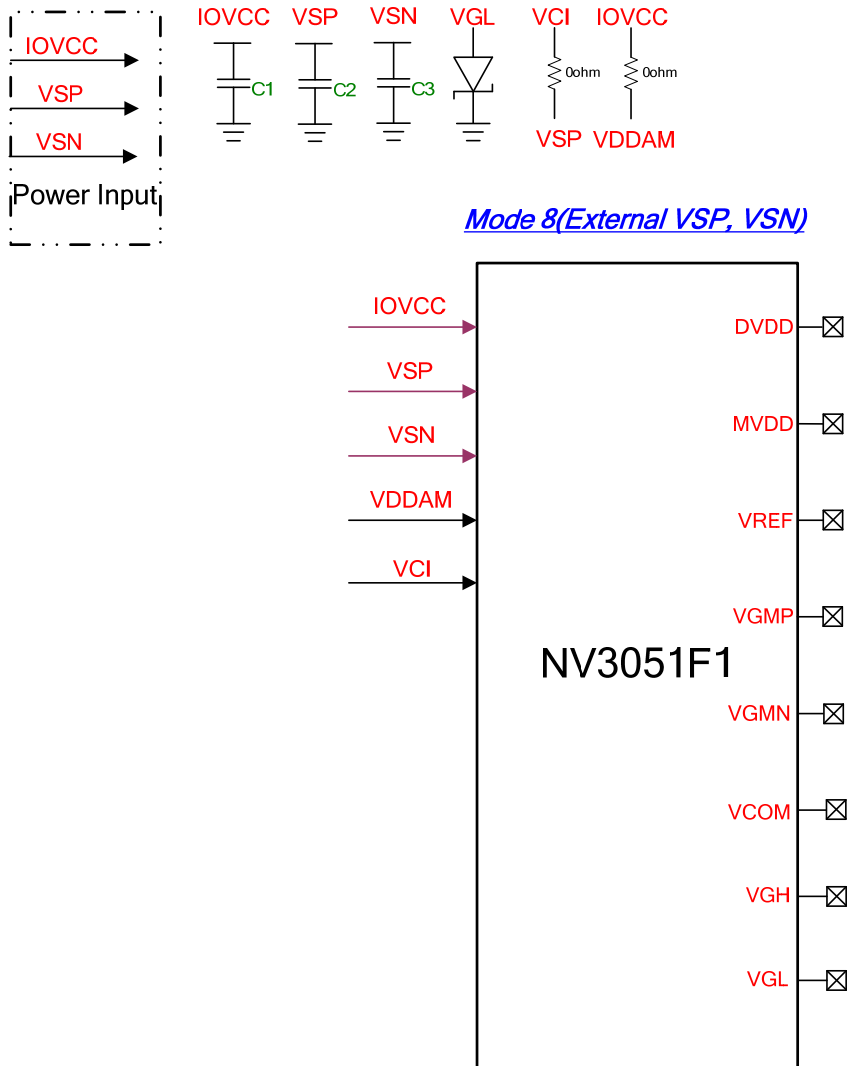


Fig 4.2

## 4.4 BOM List

### 4.4.1. Mode-3: Power IC mode

NV3051F1 BOM Lists for WXGA				
No.	Signal name	Values	Max ability	Note
1	IOVCC(C1)	1.0uF	4V	I/O and Digital Power
2	VCI(C2)	2.2uF	6.3V	Analog Power
3	C5(C3P/C3N)	1.0uF	6.3V	NV7052 related
4	C6(C2P/C2N)	1.0uF	6.3V	
5	C7(C1P/C1N)	1.0uF	6.3V	
6	VSN(C3)	2.2uF	6.3V	
7	VSP(C4)	2.2uF	6.3V	
8	VGL(D1)	schottky diode		GND-VGL diode

Note: Larger VSP/VSN component values are proposed to get better power efficiency and stability.

### 4.4.2. Mode-8: External VSP and VSN

NV3051F1 BOM Lists for WXGA (External VSP and VSN)				
No.	Signal name	Values	Max ability	Note
1	IOVCC(C1)	1.0uF	4V	I/O and Digital Power
2	VSP(C2)	2.2uF	6.3V	Analog Power
3	VSN(C3)	2.2uF	6.3V	Analog Power
4	VGL(D1)	schottky diode		GND-VGL diode

Note: Larger VSP/VSN component values are proposed to get better power efficiency and stability.

## 5.INSTRUCTIONS

### 5.1. Outline

The NV3051F1 supports high speed serial interface, MIPI to configure the system via accessing command registers. While accessing the command registers, the information that indicates which register would be accessed should be sent first. After that, the new value can be updated via system interface. The MIPI-DSI is compliant with MIPI Alliance Standard for Display Serial Interface (DSI), Version 1.01.00 and D-PHY Version 1.00.00. Updating command instructions can also be accomplished by using all supporting system interfaces .

The NV3051F1 has the following major categories of instructions:

- (1). System function instructions (User Command Set).
- (2). Customer Command List and Description (Manufacturer Command Set / Command 2).

Since updating these instructions are asynchronous to the internal clock of the NV3051F1, the updating procedure will require no waiting cycles. Furthermore, the updating procedure will not interfere with the processing of the host controller, this makes instructions can be handled smoothly and efficiently.

The following contents of this chapter will describe the supported instructions in detail.

System function commands

After the H/W reset by RESX pin or S/W reset by SWRESET command, each internal register will return to the default state (Please refer to “RESET TABLE” section). The commands 10h, 11h, 20h, 21h, 22h, 23h, 28h, 29h, 36h will be updated only during V-sync periods while module is in the “Sleep Out” mode to avoid abnormal visual effects, and will be updated immediately in the “Sleep In” mode. The Read Display Power Mode (0Ah), Read Display MADCTL (0Bh), Read Display Pixel Format (0Ch), Read Display Image Mode (0Dh), Read Display Signal Mode (0Eh), and Read Display Self Diagnostic Result (0Fh) will be updated immediately in both “Sleep In” and “Sleep Out” mode.

System function command accessing flow is described as the following example.

Example 1: Sleep Out  
CMDWR 0x11

Example 2: Display On  
CMDWR 0x29

Example 3: TE ON  
CMDWR 0x35  
DATWR 0x00

System Function Command List

Page 0 Command													
Instruction	DCX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
NOP	0	↑	1	0	0	0	0	0	0	0	0	00h	No operation
	1	1	↑	rd_00[7:0]								ffh	-
	1	1	↑	rd_01[7:0]								ffh	-
SWRESET	0	↑	1	0	0	0	0	0	0	0	1	01h	Software reset
	1	1	↑	rd_01[7:0]								ffh	-
RDDIDIF	0	↑	1	0	0	0	0	0	1	0	0	04h	Read display ID
	1	1	↑	ID1								30h	ID1 read
	1	1	↑	ID2								52h	ID2 read
	1	1	↑	ID3								01h	ID3 read
RDDPM	0	↑	1	0	0	0	0	1	0	1	0	0Ah	read display power mode
	1	1	↑	boot	idle_mode_on	0	sleep_out	normal	disp_on	0	0	08h	-
RDD MADCTL	0	↑	1	0	0	0	0	1	0	1	1	0Bh	read display MADCTL
	1	1	↑	0	0	0	0	bgr	0	ss	gs	00h	-
RDDCOLMOD	0	↑	1	0	0	0	0	1	1	0	0	0Ch	read display pixel format
	1	1	↑	0	dpi[2:0]			0	0	0	0	70h	-
RDDIM	0	↑	1	0	0	0	0	1	1	0	1	0Dh	Read display image
	1	1	↑	0	0	inver_on	pixel_on	pixel_off	gcs[2:0]			00h	-
RDDSM	0	↑	1	0	0	0	0	1	1	1	0	0Eh	Read display signal mode
	1	1	↑	tear_on	tear_mode	0	0	0	0	0	0	00h	-
RDDSDR	0	↑	1	0	0	0	0	1	1	1	1	0Fh	Read display self-diagnostic result
	1	1	↑	regld	fundt	0	0	0	0	0	esd_c hk	00h	-
SLPIN	0	↑	1	0	0	0	1	0	0	0	0	10h	Sleep in
SLPOUT	0	↑	1	0	0	0	1	0	0	0	1	11h	Sleep out
NORON	0	↑	1	0	0	0	1	0	0	1	1	13h	normal mode on and partial mode off
INVOFF	0	↑	1	0	0	1	0	0	0	0	0	20h	Display inversion off
INVON	0	↑	1	0	0	1	0	0	0	0	1	21h	Display inversion on
ALLPOFF	0	↑	1	0	0	1	0	0	0	1	0	22h	All Pixel off
ALLPON	0	↑	1	0	0	1	0	0	0	1	1	23h	All Pixel on
DISPOFF	0	↑	1	0	0	1	0	1	0	0	0	28h	Display off

Page 0 Command													
Instruction	DCX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
DISPON	0	↑	1	0	0	1	0	1	0	0	1	29h	Display on
TEOFF	0	↑	1	0	0	1	1	0	1	0	0	34h	Tearing Effect Line off
TEON	0	↑	1	0	0	1	1	0	1	0	1	35h	Tearing Effect Line on
	1	↑	1	0	0	0	0	0	0	0	tear_m ode	00h	-
MADCTL	0	↑	1	0	0	1	1	0	1	1	0	36h	Memory data access control
	1	↑	1	0	0	0	0	bgr	0	ss	gs	00h	-
IDMODEOFF	0	↑	1	0	0	1	1	1	0	0	0	38h	Idle mode off
IDMODEON	0	↑	1	0	0	1	1	1	0	0	1	39h	Idle mode on and other mode off
WRTE SCN	0	↑	1	0	1	0	0	0	1	0	0	44h	Write tear scanline
	1	↑	1	te_on_lines[7:0]								00h	-
RDSCNL	0	↑	1	0	1	0	0	0	1	0	1	45h	Read scanline
	1	1	↑	te_on_lines[7:0]								00h	-
WRTEWIDTH	0	↑	1	0	1	0	0	0	1	1	0	46h	Write Tear Scan Line Width
	1	↑	1	te_width[7:0]								00h	-
RDTEWIDTH	0	↑	1	0	1	0	0	0	1	1	1	47h	Read Tear Scan Line Width
	1	1	↑	te_width[7:0]								00h	-
WRDISBV	0	↑	1	0	1	0	1	0	0	0	1	51h	Write Display Brightness
	1	↑	1	dbv__reg[15:8]								00h	-
	1	↑	1	dbv__reg[7:0]								00h	-
RDDISBV	0	↑	1	0	1	0	1	0	0	1	0	52h	Read Display Brightness
	1	1	↑	dbv[7:0]								00h	-
WRCTRLD	0	↑	1	0	1	0	1	0	0	1	1	53h	Write CTRL Display
	1	↑	1	sam_o utdoor 3	0	bctrl	0	disp_di m	backlight _on	0	0	00h	-
RDCTRLD	0	↑	1	0	1	0	1	0	1	0	0	54h	Read CTRL Display Value
	1	1	↑	0	0	bctrl	0	disp_di m	backlight _on	0	0	00h	-

Page 0 Command													
Instruction	DCX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
RDID1	0	↑	1	1	1	0	1	1	0	1	0	DAh	read display id 1
	1	1	↑	id1								30h	-
RDID2	0	↑	1	1	1	0	1	1	0	1	1	DBh	read display id 2
	1	1	↑	id2								52h	-
RDID3	0	↑	1	1	1	0	1	1	1	0	0	DCh	read display id 3
	1	1	↑	id3								01h	-
ENEXTC	0	↑	1	1	1	1	1	1	1	1	1	FFh	EXTC Command Set Enable Register
	1	↑	1	0	0	0	0	0	0	page[1:0]		00h	-



## 5.2. SYSTEM COMMAND DESCRIPTION

### 5.2.1. NOP (00h)

00H		NOP (No Operation)																						
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	Default														
Command	Write	0	0	0	0	0	0	0	0	00H														
1 <sup>st</sup> Parameter	Read	rd_00[7:0]								ffh														
2 <sup>nd</sup> Parameter	Read	rd_01[7:0]								ffh														
Description	rd_00[7:0]:Support MOTO E4 ID1 read function. rd_01[7:0]:Usually apply to software reset order.After finish to send “FF 98 81 01”,it can be used as MOTE E4 ID2 read address.																							
Restriction	-																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On,Sleep Out	Yes	Sleep Out	Yes	Sleep In	Yes						
Status	Availability																							
Normal Mode On,Sleep Out	Yes																							
Sleep Out	Yes																							
Sleep In	Yes																							
Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="2">Default Value</th> </tr> <tr> <th>rd_00[7:0]</th> <th>rd_01[7:0]</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>ffh</td> <td>ffh</td> </tr> <tr> <td>S/W Reset</td> <td>ffh</td> <td>ffh</td> </tr> <tr> <td>H/W Reset</td> <td>ffh</td> <td>ffh</td> </tr> </tbody> </table>										Status	Default Value		rd_00[7:0]	rd_01[7:0]	Power On Sequence	ffh	ffh	S/W Reset	ffh	ffh	H/W Reset	ffh	ffh
Status	Default Value																							
	rd_00[7:0]	rd_01[7:0]																						
Power On Sequence	ffh	ffh																						
S/W Reset	ffh	ffh																						
H/W Reset	ffh	ffh																						

5.2.2. Software Reset(01h)

01H		SWRESET (Software Reset)																
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	Default								
Command	Write	0	0	0	0	0	0	0	1	01H								
Parameter	Write/Read	rd_01[7:0]								ffh								
Description	rd_01[7:0]:Usually apply to software reset order.After finish to send “FF 98 81 01”,it can be used as MOTE E4 ID2 read address.																	
Restriction	It is necessary to wait 5msec before sending a new command following software reset.The display module loads all display suppliers’ factory default values to the registers during 5msec.If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep Out command.The Software Reset command cannot be sent during Sleep Out sequence. As MOTE E4 ID2 Read restriction, It can be to read after send“FF 98 81 01”.																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On,Sleep Out	Yes	Sleep Out	Yes	Sleep In	Yes
Status	Availability																	
Normal Mode On,Sleep Out	Yes																	
Sleep Out	Yes																	
Sleep In	Yes																	
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>ffh</td> </tr> <tr> <td>S/W Reset</td> <td>ffh</td> </tr> <tr> <td>H/W Reset</td> <td>ffh</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	ffh	S/W Reset	ffh	H/W Reset	ffh
Status	Default Value																	
Power On Sequence	ffh																	
S/W Reset	ffh																	
H/W Reset	ffh																	

5.2.3 Read Display ID(04h)

04H		RDDIDIF (Read Display ID)																											
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	Default																			
Command	Write	0	0	0	0	0	1	0	0	04H																			
1 <sup>st</sup> parameter	Read	ID1								30h																			
2 <sup>nd</sup> parameter	Read	ID2								52h																			
3 <sup>rd</sup> parameter	Read	ID3								01h																			
Description	The 1 <sup>st</sup> parameter (ID1): LCD module's manufacturer ID. The 2 <sup>nd</sup> parameter (ID2): LCD module/driver version ID. The 3 <sup>rd</sup> parameter (ID3): LCD module/driver ID. Commands RDID1/2/3(DAh, DBh, DCh) read data correspond to the parameters 1,2,3 of the command 04h, respectively.																												
Restriction																													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes							
Status	Availability																												
Normal Mode On, Idle Mode Off, Sleep Out	Yes																												
Normal Mode On, Idle Mode On, Sleep Out	Yes																												
Partial Mode On, Idle Mode Off, Sleep Out	Yes																												
Partial Mode On, Idle Mode On, Sleep Out	Yes																												
Sleep In	Yes																												
Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="3">Default Value</th> </tr> <tr> <th>ID1</th> <th>ID2</th> <th>ID3</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>30h</td> <td>52h</td> <td>01h</td> </tr> <tr> <td>S/W Reset</td> <td>30h</td> <td>52h</td> <td>01h</td> </tr> <tr> <td>H/W Reset</td> <td>30h</td> <td>52h</td> <td>01h</td> </tr> </tbody> </table>										Status	Default Value			ID1	ID2	ID3	Power On Sequence	30h	52h	01h	S/W Reset	30h	52h	01h	H/W Reset	30h	52h	01h
Status	Default Value																												
	ID1	ID2	ID3																										
Power On Sequence	30h	52h	01h																										
S/W Reset	30h	52h	01h																										
H/W Reset	30h	52h	01h																										
Flow Chart	<div style="display: flex; justify-content: space-around;"> <div style="text-align: center;"> <p>Serial I/F Mode</p> </div> <div style="text-align: center;"> <p>Parallel I/F Mode</p> </div> </div> <div style="margin-top: 10px;"> <p><b>Legend</b></p> <ul style="list-style-type: none"> <li>Command (Rectangle)</li> <li>Parameter (Parallelogram)</li> <li>Display (Oval)</li> <li>Action (Hexagon)</li> <li>Mode (Oval)</li> <li>Sequential transfer (Wavy arrow)</li> </ul> </div>																												

5.2.4. Read Display Power Mode(0Ah)

0AH		RDDPM (Read Display Power Mode)																
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	Default								
Command	Write	0	0	0	0	1	0	1	0	0Ah								
parameter	Read	boost	idle_m ode_on	0	sleep_out	normal	disp_on	0	0	08h								
Description	<p>boost=0, charge pump booster off mode.                      boost=1, charge pump booster on mode.                      sleep_out=0,Sleep In Mode.                      sleep_out=1,Sleep Out Mode.                      normal =0,Display Normal Mode Off.                      normal =1,Display Normal Mode On.                      disp_on=0,Display is Off.                      disp_on =1, Display is On.                      idle_mode_on=0: idel mode off.                      idle_mode_on=1: idel mode on.                      This read byte can programmed by OTP Function.</p>																	
Restriction	-																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On,Sleep Out	Yes	Sleep Out	Yes	Sleep In	Yes
Status	Availability																	
Normal Mode On,Sleep Out	Yes																	
Sleep Out	Yes																	
Sleep In	Yes																	
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>8'h08</td> </tr> <tr> <td>S/W Reset</td> <td>8'h08</td> </tr> <tr> <td>H/W Reset</td> <td>8'h08</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	8'h08	S/W Reset	8'h08	H/W Reset	8'h08
Status	Default Value																	
Power On Sequence	8'h08																	
S/W Reset	8'h08																	
H/W Reset	8'h08																	

5.2.5. Read Display MADCTL(0BH)

0BH		RDDMADCTL(Read Display MADCTL)																
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	Default								
Command	Write	0	0	0	0	1	0	1	1	0BH								
Parameter	Read	0	0	0	0	bgr	0	ss	gs	00H								
Description	This command indicates the current status of the display: bgr=0,RGB format. bgr=1,BGR format. ss=0,Source output Left to Right. ss=1,Source output Right to Left. gs=0,Gate output from top to bottom. gs=1,Gate output from bottom to top.																	
Restriction	-																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On,Sleep Out	Yes	Sleep Out	Yes	Sleep In	Yes
Status	Availability																	
Normal Mode On,Sleep Out	Yes																	
Sleep Out	Yes																	
Sleep In	Yes																	
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>8'h00</td> </tr> <tr> <td>S/W Reset</td> <td>8'h00</td> </tr> <tr> <td>H/W Reset</td> <td>8'h00</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	8'h00	S/W Reset	8'h00	H/W Reset	8'h00
Status	Default Value																	
Power On Sequence	8'h00																	
S/W Reset	8'h00																	
H/W Reset	8'h00																	


5.2.6. Read Display Pixel Format(0CH)

0CH		RDDCOLMOD (Read Display COLMOD)								
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	0	0	0	1	1	0	0	0CH
Parameter	Read	0	dpi[2:0]			0	0	0	0	70H
Description	This command indicates the current status of the display as described in the table below:									
	dpi[2:0]			Interface Format						
	1	0	1	16-bit/pixel						
	1	1	0	18-bit/pixel						
	1	1	1	24-bit/pixel						
Others			Reserved							
Restriction	-									
Register Availability	Status		Availability							
	Normal Mode On,Sleep Out		Yes							
	Sleep Out		Yes							
	Sleep In		Yes							
Default	Status		Default Value							
	Power On Sequence		8'h70							
	S/W Reset		8'h70							
	H/W Reset		8'h70							

5.2.7. Read Display Image Mode(0DH)

0DH		RDDIM (Read Display Image Mode)																
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	Default								
Command	Write	0	0	0	0	1	1	0	1	0DH								
parameter	Read	0	0	inver_on	pixel_on	pixel_off	gcs[2:0]			00H								
Description	inver_on =0,Inversion is Off. inver_on =1,Inversion is On. pixel_on =0,Normal Display. pixel_on =1,White Display. pixel_off =0,Normal Display. pixel_off =1,Black Display. GCS=3'b000,GC0 is selected,others are not defined.																	
Restriction	-																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On,Sleep Out	Yes	Sleep Out	Yes	Sleep In	Yes
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Sleep Out	Yes																	
Sleep In	Yes																	
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Status	Default Value																	
Power On Sequence	8'h00																	
S/W Reset	8'h00																	
H/W Reset	8'h00																	

5.2.8. Read Display Signal Mode(0EH)

0EH		RDDSM (Read Display Signal Mode)																
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	Default								
Command	Write	0	0	0	0	1	1	1	0	0Eh								
Parameter	Read	tear_on	tear_mode	0	0	0	0	0	0	00h								
Description	This command indicates the current status of the display. TEON=0, Tearing Effect Line Off. TEON=1, Tearing Effect Line On. TEAR_MODE=0, The Tearing Effect Output line consists of V-Blanking information only.																	
	 <p>Vertical time scale</p> <p>Vertical time scale</p>																	
Restriction	-																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Sleep Out	Yes	Sleep Out	Yes	Sleep In	Yes								
	Status	Availability																
	Normal Mode On, Sleep Out	Yes																
	Sleep Out	Yes																
Sleep In	Yes																	
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	Status	Default Value																
	Power On Sequence	8'h00																
S/W Reset	8'h00																	
H/W Reset	8'h00																	



5.2.9. Read Display Self-Diagnostic Result(0FH)

0FH		RDDSDR ( Read Display Self-Diagnostic Result )								
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	0	0	0	1	1	1	1	0FH
Parameter	Read	regld	fundt	0	0	0	0	0	esd_c hk	00h
Description	regld =1,when the OTP and register values are the same. fundt =1,when the chip met User's functionality requirements. esd_chk: ESD check result.									
Restriction	-									
Register Availability			<b>Status</b>		<b>Availability</b>					
			Normal Mode On,Sleep Out		Yes					
			Sleep Out		Yes					
			Sleep In		Yes					
Default			<b>Status</b>		<b>Default Value</b>					
			Power On Sequence		8'h00					
			S/W Reset		8'h00					
			H/W Reset		8'h00					

5.2.10. Sleep In(10h)

10H		SLPIN (Sleep In)																
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	Default								
Command	Write	0	0	0	1	0	0	0	0	10H								
Parameter	-	No Parameter								-								
Description	This command cause the NV3051F1 to enter the minimum power consumption mode. In this mode the NV3051F1 control signals,Internal oscillator and panel scanning are stopped.																	
Restriction	This command has no effect when module is already in Sleep In mode. Sleep In Mode can only be left by the Sleep Out command. It is necessary to wait 5msec before sending the next command; this is to allow time for the supply voltages and clock circuits to stabilize. It is necessary to wait 120msec after sending Sleep Out command(when in Sleep In Mode)before the Sleep In command can be sent.																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On,Sleep Out	Yes	Sleep Out	Yes	Sleep In	Yes
Status	Availability																	
Normal Mode On,Sleep Out	Yes																	
Sleep Out	Yes																	
Sleep In	Yes																	
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Sleep In Mode</td> </tr> <tr> <td>S/W Reset</td> <td>Sleep In Mode</td> </tr> <tr> <td>H/W Reset</td> <td>Sleep In Mode</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	Sleep In Mode	S/W Reset	Sleep In Mode	H/W Reset	Sleep In Mode
Status	Default Value																	
Power On Sequence	Sleep In Mode																	
S/W Reset	Sleep In Mode																	
H/W Reset	Sleep In Mode																	

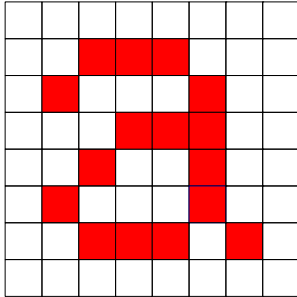
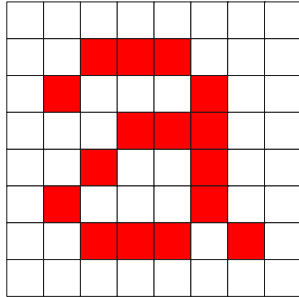
5.2.11. Sleep Out(11H)

11H		SLPOUT (Sleep Out)																
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	Default								
Command	Write	0	0	0	1	0	0	0	1	11H								
Parameter	-	No Parameter								-								
Description	This command turns off sleep mode. In this mode ,the NV3051F1 control signals,Internal oscillator and panel scanning are started.																	
Restriction	This command has no effect when module is already in Sleep Out mode. Sleep Out mode can be left by the Sleep In command(10h),S/W reset command (01h) or H/W reset. It is necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize. The NV3051F1 loads all display supplier’s factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the NV3051F1 is already Sleep Out mode.During this 5msec, NV3051F1 is running self-diagnostic functions. It is necessary to wait 120msec after sending the Sleep In command (when in Sleep Out mode) before the Sleep Out command can be sent.																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On,Sleep Out	Yes	Sleep Out	Yes	Sleep In	Yes
Status	Availability																	
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Status	Default Value																	
Power On Sequence	Sleep In Mode																	
S/W Reset	Sleep In Mode																	
H/W Reset	Sleep In Mode																	

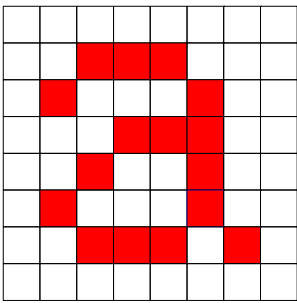
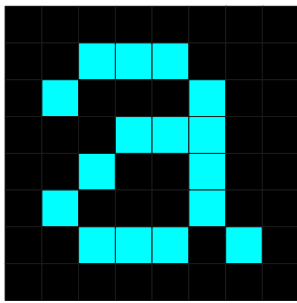
5.2.12. Normal Display Mode On(13H)

13H		NORON (Normal Display Mode On)																
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	Default								
Command	Write	0	0	0	1	0	0	1	1	13H								
Parameter	-	No Parameter								-								
Description	This command returns the display to Normal Display Mode.																	
Restriction	This command has no effect when Normal Display Mode is active.																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On,Sleep Out	Yes	Sleep Out	Yes	Sleep In	Yes
Status	Availability																	
Normal Mode On,Sleep Out	Yes																	
Sleep Out	Yes																	
Sleep In	Yes																	
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Normal Display Mode On.</td> </tr> <tr> <td>S/W Reset</td> <td>Normal Display Mode On.</td> </tr> <tr> <td>H/W Reset</td> <td>Normal Display Mode On.</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	Normal Display Mode On.	S/W Reset	Normal Display Mode On.	H/W Reset	Normal Display Mode On.
Status	Default Value																	
Power On Sequence	Normal Display Mode On.																	
S/W Reset	Normal Display Mode On.																	
H/W Reset	Normal Display Mode On.																	

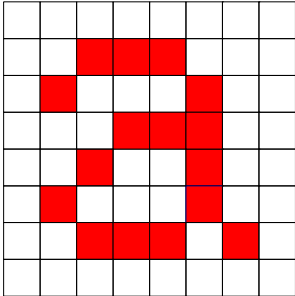

5.2.13. Display Inversion Off(20H)

20H	INVOFF (Display Inversion Off )																	
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	Default								
Command	Write	0	0	1	0	0	0	0	0	20H								
Parameter	-	No Parameter								-								
Description	<p>This command is used to recover from display inversion On mode. This command does not change any other status.</p> <div style="display: flex; justify-content: space-around; align-items: center;"> <div style="text-align: center;"> <p>Before</p>  </div> <div style="font-size: 2em;">→</div> <div style="text-align: center;"> <p>After</p>  </div> </div>																	
Restriction	This command has no effect when module is already in Display Inversion Off mode.																	
Register Availability	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On,Sleep Out	Yes	Sleep Out	Yes	Sleep In	Yes
Status	Availability																	
Normal Mode On,Sleep Out	Yes																	
Sleep Out	Yes																	
Sleep In	Yes																	
Default	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display Inversion Off</td> </tr> <tr> <td>S/W Reset</td> <td>Display Inversion Off</td> </tr> <tr> <td>H/W Reset</td> <td>Display Inversion Off</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	Display Inversion Off	S/W Reset	Display Inversion Off	H/W Reset	Display Inversion Off
Status	Default Value																	
Power On Sequence	Display Inversion Off																	
S/W Reset	Display Inversion Off																	
H/W Reset	Display Inversion Off																	

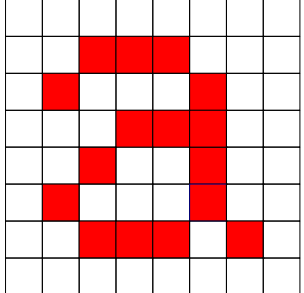
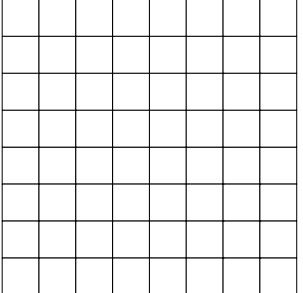
5.2.14. Display Inversion On(21H)

21H	INVON (Display Inversion On )																	
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	Default								
Command	Write	0	0	1	0	0	0	0	1	21H								
Parameter	-	No Parameter								-								
Description	<p>This command is used to enter into Display Inversion On mode.                      This command does not change any other status.                      To exit Display Inversion On mode, the Display Inversion Off command(20h)should be written.</p> <div style="display: flex; justify-content: space-around; align-items: center;"> <div style="text-align: center;"> <p>Before</p>  </div> <div style="font-size: 2em;">→</div> <div style="text-align: center;"> <p>After</p>  </div> </div>																	
Restriction	This command has no effect when the NV3051F1 is already in Inversion On mode.																	
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%;">Status</th> <th style="width: 50%;">Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On,Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Sleep In</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On,Sleep Out	Yes	Sleep Out	Yes	Sleep In	Yes
Status	Availability																	
Normal Mode On,Sleep Out	Yes																	
Sleep Out	Yes																	
Sleep In	Yes																	
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%;">Status</th> <th style="width: 50%;">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td style="text-align: center;">Display Inversion Off</td> </tr> <tr> <td>S/W Reset</td> <td style="text-align: center;">Display Inversion Off</td> </tr> <tr> <td>H/W Reset</td> <td style="text-align: center;">Display Inversion Off</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	Display Inversion Off	S/W Reset	Display Inversion Off	H/W Reset	Display Inversion Off
Status	Default Value																	
Power On Sequence	Display Inversion Off																	
S/W Reset	Display Inversion Off																	
H/W Reset	Display Inversion Off																	

5.2.15. All Pixel Off(22H)

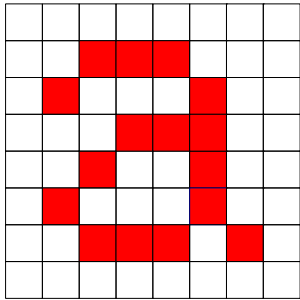
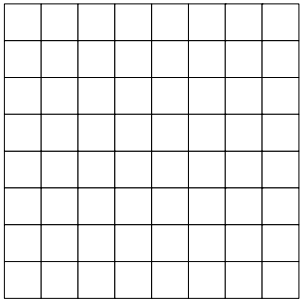
22H		ALLPOFF (All Pixels Off)																
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	Default								
Command	Write	0	0	1	0	0	0	1	0	22H								
Parameter	-	No Parameter								-								
Description	<p>This command turns the display panel black in ‘Sleep Out’ mode and a status of the ‘Display On/Off’ register can be ‘on’ or ‘off’.</p> <p>This command does not change any other status.</p> <div style="display: flex; justify-content: space-around; align-items: center;"> <div style="text-align: center;"> <p>Before</p>  </div> <div style="font-size: 2em;">→</div> <div style="text-align: center;"> <p>After</p>  </div> </div> <p>‘All Pixels On’, ‘Normal Display Mode On’ commands are used to leave this mode.</p> <p>0:normal display                      1:NB screen:nom_black = 0,black display;nom_black = 1,white display                      NW screen:nom_black = 0,white display;nom_black = 1,black display</p>																	
Restriction	This command has no effect when the NV3051F1 is already in All Pixels Off mode.																	
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%;">Status</th> <th style="width: 50%;">Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On,Sleep Out	Yes	Sleep Out	Yes	Sleep In	Yes
Status	Availability																	
Normal Mode On,Sleep Out	Yes																	
Sleep Out	Yes																	
Sleep In	Yes																	
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%;">Status</th> <th style="width: 50%;">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Off</td> </tr> <tr> <td>S/W Reset</td> <td>Off</td> </tr> <tr> <td>H/W Reset</td> <td>Off</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	Off	S/W Reset	Off	H/W Reset	Off
Status	Default Value																	
Power On Sequence	Off																	
S/W Reset	Off																	
H/W Reset	Off																	

5.2.16. All Pixels On(23H)

23H		ALLPON (All Pixels On)																
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	Default								
Command	Write	0	0	1	0	0	0	1	1	23H								
Parameter	-	No Parameter								-								
Description	<p>This command turns the display panel white in ‘Sleep out ’ mode and a status of the ‘Display On/Off’ register can be ‘on’ or ‘off’.This command does not change any other status.</p>																	
	<div style="display: flex; justify-content: space-around; align-items: center;"> <div style="text-align: center;"> <p>Before</p>  </div> <div style="font-size: 2em; margin: 0 20px;">→</div> <div style="text-align: center;"> <p>After</p>  </div> </div> <p>‘All Pixels Off’, ‘Normal Display Mode On’ commands are used to leave this mode.                      0:normal display.                      1:NB screen:nom_black = 0,white display;nom_black = 1,black display.                      NW screen:nom_black = 0,black display;nom_black = 1,white display.</p>																	
Restriction	This command has no effect when the NV3051F1 is already in All Pixels On mode.																	
Register Availability	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On,Sleep Out	Yes	Sleep Out	Yes	Sleep In	Yes
Status	Availability																	
Normal Mode On,Sleep Out	Yes																	
Sleep Out	Yes																	
Sleep In	Yes																	
Default	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Off</td> </tr> <tr> <td>S/W Reset</td> <td>Off</td> </tr> <tr> <td>H/W Reset</td> <td>Off</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	Off	S/W Reset	Off	H/W Reset	Off
Status	Default Value																	
Power On Sequence	Off																	
S/W Reset	Off																	
H/W Reset	Off																	



5.2.17. Display Off(28H)

28H		DISOFF (Display Off)																
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	Default								
Command	Write	0	0	1	0	1	0	0	0	28H								
Parameter	-	No Parameter								-								
Description	<p>This command is used to enter into Display Off mode. In this mode, the output data is disabled and blank page is inserted.</p> <p>This command makes no change any other status.</p> <p>There will be no abnormal visible effect on the display.</p> <div style="display: flex; justify-content: space-around; align-items: center;"> <div style="text-align: center;"> <p><b>Before</b></p>  </div> <div style="font-size: 2em;">→</div> <div style="text-align: center;"> <p><b>After</b></p>  </div> </div>																	
Restriction	This command has no effect when module is already in Display Off mode.																	
Register Availability	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On,Sleep Out	Yes	Sleep Out	Yes	Sleep In	Yes
Status	Availability																	
Normal Mode On,Sleep Out	Yes																	
Sleep Out	Yes																	
Sleep In	Yes																	
Default	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display off</td> </tr> <tr> <td>S/W Reset</td> <td>Display off</td> </tr> <tr> <td>H/W Reset</td> <td>Display off</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	Display off	S/W Reset	Display off	H/W Reset	Display off
Status	Default Value																	
Power On Sequence	Display off																	
S/W Reset	Display off																	
H/W Reset	Display off																	

5.2.18. Display On(29H)

29H		DISON (Display On)																
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	Default								
Command	Write	0	0	1	0	1	0	0	1	29H								
Parameter	-	No Parameter								-								
Description	<p>This command is used to recover from Display Off mode. Output data is enabled. This command does not change any other status.</p> <div style="display: flex; justify-content: space-around; align-items: center;"> <div style="text-align: center;"> <p><b>Before</b></p> </div> <div style="font-size: 2em;">→</div> <div style="text-align: center;"> <p><b>After</b></p> </div> </div>																	
Restriction	This command has no effect when the NV3051F1 is already in Display on mode.																	
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%;">Status</th> <th style="width: 50%;">Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On,Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Sleep In</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On,Sleep Out	Yes	Sleep Out	Yes	Sleep In	Yes
Status	Availability																	
Normal Mode On,Sleep Out	Yes																	
Sleep Out	Yes																	
Sleep In	Yes																	
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%;">Status</th> <th style="width: 50%;">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td style="text-align: center;">Display off</td> </tr> <tr> <td>S/W Reset</td> <td style="text-align: center;">Display off</td> </tr> <tr> <td>H/W Reset</td> <td style="text-align: center;">Display off</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	Display off	S/W Reset	Display off	H/W Reset	Display off
Status	Default Value																	
Power On Sequence	Display off																	
S/W Reset	Display off																	
H/W Reset	Display off																	

5.2.19. Tearing Effect Line OFF(34H)

34H		TEOFF (Tearing Effect Line OFF)																
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	Default								
Command	Write	0	0	1	1	0	1	0	0	34H								
Parameter	-	No Parameter								-								
Description	This command is used to turn off the Display module's Tearing Effect output signal(Active Low) from the TE signal line.																	
Restriction	This command has no effect when the Tearing Effect output is already off.																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On,Sleep Out	Yes	Sleep Out	Yes	Sleep In	Yes
	Status	Availability																
	Normal Mode On,Sleep Out	Yes																
	Sleep Out	Yes																
Sleep In	Yes																	
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Tearing Effect Line Off</td> </tr> <tr> <td>S/W Reset</td> <td>Tearing Effect Line Off</td> </tr> <tr> <td>H/W Reset</td> <td>Tearing Effect Line Off</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	Tearing Effect Line Off	S/W Reset	Tearing Effect Line Off	H/W Reset	Tearing Effect Line Off
	Status	Default Value																
	Power On Sequence	Tearing Effect Line Off																
	S/W Reset	Tearing Effect Line Off																
H/W Reset	Tearing Effect Line Off																	

5.2.20. Tearing Effect Line ON(35H)

35H		TEON (Tearing Effect Line On)																
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	Default								
Command	Write	0	0	1	1	0	1	0	1	35H								
Parameter	-	No Parameter							tear_mode	00H								
Description	This command is used to turn on the Tearing Effect output signal from the TE signal line. tear_mode:describes the mode of the Tearing Effect Output Line. Tearing Effect Line mode. 0:The Tearing Effect Output line consists of V-Blanking information only. 1:The Tearing Effect Output line consists of both V-Blanking and H-Blanking information.																	
Restriction	This command has no effect when the Tearing Effect output is already on.																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On,Sleep Out	Yes	Sleep Out	Yes	Sleep In	Yes
Status	Availability																	
Normal Mode On,Sleep Out	Yes																	
Sleep Out	Yes																	
Sleep In	Yes																	
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Tearing Effect Line Off</td> </tr> <tr> <td>S/W Reset</td> <td>Tearing Effect Line Off</td> </tr> <tr> <td>H/W Reset</td> <td>Tearing Effect Line Off</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	Tearing Effect Line Off	S/W Reset	Tearing Effect Line Off	H/W Reset	Tearing Effect Line Off
Status	Default Value																	
Power On Sequence	Tearing Effect Line Off																	
S/W Reset	Tearing Effect Line Off																	
H/W Reset	Tearing Effect Line Off																	

5.2.21. Display Access Control(36H)

36H		MADCTL (Display Access Control)								
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	0	1	1	0	1	1	0	36H
Parameter	Write	0	0	0	0	bgr	0	ss	gs	00h
Description	This command defines the panel operation mode.									
	<b>SYMBOL</b>	<b>NAME</b>			<b>DESCRIPTION</b>					
	bgr	Pannel RGB-BGR Order.			Color selector switch control. (0' =RGB color filter panel, '1' =BGR color filter panel)					
	ss	Panel Flip Horizontal.			Select the source driver scan direction on the panel module. (SS="1" Source Scan sequence from right to left, '0' = Source Scan sequence from left to right)					
gs	Panel Flip Vertical.			Select the gate driver scan direction on panel module. (GS="1" Gate Scan sequence from bottom to top, '0' = Gate Scan sequence from top to bottom)						
Note:gs scan direction depend on panel's design. Top-Left(0,0) means the physical panel location.										
Restriction	-									
Register Availability			<b>Status</b>		<b>Availability</b>					
			Normal Mode On,Sleep Out		Yes					
			Sleep Out		Yes					
			Sleep In		Yes					
Default			<b>Status</b>		<b>Default Value</b>					
			Power On Sequence		8'h00					
			S/W Reset		8'h00					
			H/W Reset		8'h00					

5.2.22. Idle Mode Off(38H)

38H		IDMODEOFF (Idle Mode Off)																
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	Default								
Command	Write	0	0	1	1	1	0	0	0	38H								
Parameter	-	No Parameter								-								
Description	This command causes the Display module to exit the Idle mode. In the Idle Mode Off, the display panel can display a maximum of 16.7M colors.																	
Restriction	This command has no effect when the module is already in the Idle Mode Off.																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On,Idle Mode Off,Sleep Out	Yes	Normal Mode On,Idle Mode On,Sleep Out	Yes	Sleep In	Yes
Status	Availability																	
Normal Mode On,Idle Mode Off,Sleep Out	Yes																	
Normal Mode On,Idle Mode On,Sleep Out	Yes																	
Sleep In	Yes																	
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Idle Mode Off</td> </tr> <tr> <td>S/W Reset</td> <td>Idle Mode Off</td> </tr> <tr> <td>H/W Reset</td> <td>Idle Mode Off</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	Idle Mode Off	S/W Reset	Idle Mode Off	H/W Reset	Idle Mode Off
Status	Default Value																	
Power On Sequence	Idle Mode Off																	
S/W Reset	Idle Mode Off																	
H/W Reset	Idle Mode Off																	

5.2.23. Idle mode on and other mode off (39H)

39H		IDMODEON (Idle mode on and other mode off)																
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	Default								
Command	Write	0	0	1	1	1	0	0	1	39H								
Parameter	-	No Parameter								-								
Description	This command is used to enter into the Idle Mode On. In the Idle Mode On, color expression is reduced.																	
Restriction	This command has no effect when the module is already in the Idle Mode On.																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																	
Normal Mode On, Idle Mode Off, Sleep Out	Yes																	
Normal Mode On, Idle Mode On, Sleep Out	Yes																	
Sleep In	Yes																	
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Idle Mode Off</td> </tr> <tr> <td>S/W Reset</td> <td>Idle Mode Off</td> </tr> <tr> <td>H/W Reset</td> <td>Idle Mode Off</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	Idle Mode Off	S/W Reset	Idle Mode Off	H/W Reset	Idle Mode Off
Status	Default Value																	
Power On Sequence	Idle Mode Off																	
S/W Reset	Idle Mode Off																	
H/W Reset	Idle Mode Off																	

5.2.24. Write Tear Scan Line(44H)

44H		WRTE SCN (Write Tear Scan Line)								
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	1	0	0	0	1	0	0	44H
Parameter	Write	te_on_lines[7:0]								00H
Description	This command turns on the display module's TE signal when the display module reaches line te_on_lines[7:0].									
Restriction	The command takes affect with the end of one frame.									
Register Availability			<b>Status</b>		<b>Availability</b>					
			Normal Mode On,Sleep Out		Yes					
			Sleep Out		Yes					
			Sleep In		Yes					
Default			<b>Status</b>		<b>Default Value</b>					
			Power On Sequence		8'h00					
			S/W Reset		8'h00					
			H/W Reset		8'h00					



5.2.25. Read Scan Line(45H)

45H		RDSCNL(Read Scan Line)								
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	1	0	0	0	1	0	1	45H
Parameter	Read	te_on_lines[7:0]								00h
Description	This read byte returns the current scan line.									
Restriction	-									
Register Availability			<b>Status</b>				<b>Availability</b>			
			Normal Mode On,Sleep Out				Yes			
			Sleep Out				Yes			
			Sleep In				Yes			
Default			<b>Status</b>				<b>Default Value</b>			
			Power On Sequence				8'h00			
			S/W Reset				8'h00			
			H/W Reset				8'h00			

5.2.26. Write Tear Scan Line Width(46H)

46H		WRTEWIDTH(Write Tear Scan Line Width)								
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	1	0	0	0	1	1	0	46H
Parameter	Write	te_width[7:0]								00H
Description	Set the width of TE scan line.									
Restriction	-									
Register Availability			<b>Status</b>				<b>Availability</b>			
			Normal Mode On,Sleep Out				Yes			
			Sleep Out				Yes			
			Sleep In				Yes			
Default			<b>Status</b>				<b>Default Value</b>			
			Power On Sequence				8'h00			
			S/W Reset				8'h00			
			H/W Reset				8'h00			

5.2.27. Read Tear Scan Line Width(47H)

47H		RDTEWIDTH(Read Tear Scan Line Width)																
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	Default								
Command	Write	0	1	0	0	0	1	1	1	47H								
Parameter	Read	te_width[7:0]								00H								
Description	Read the width of TE scan line.																	
Restriction	-																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On,Sleep Out	Yes	Sleep Out	Yes	Sleep In	Yes
	Status	Availability																
	Normal Mode On,Sleep Out	Yes																
	Sleep Out	Yes																
Sleep In	Yes																	
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>8'h00</td> </tr> <tr> <td>S/W Reset</td> <td>8'h00</td> </tr> <tr> <td>H/W Reset</td> <td>8'h00</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	8'h00	S/W Reset	8'h00	H/W Reset	8'h00
	Status	Default Value																
	Power On Sequence	8'h00																
	S/W Reset	8'h00																
H/W Reset	8'h00																	

5.2.28. Write Display Brightness Value(51H)

51H		WRDISBV(Write Display Brightness Value)																				
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	Default												
Command	Write	0	1	0	1	0	0	0	1	51H												
1 <sup>st</sup> Parameter	Write	dbv_reg[15:8]								00H												
2 <sup>nd</sup> Parameter	Write	dbv_reg[7:0]								00H												
Description	This command is used to adjust the brightness value of the display. dbv_reg[15:0]:16-bit,for display brightness of manual brightness setting in the NV3051F1.PWM output signal sends to LEDPWM pin to control the LED driver IC in order to control display brightness.																					
Restriction	-																					
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On,Sleep Out	Yes	Sleep Out	Yes	Sleep In	Yes				
Status	Availability																					
Normal Mode On,Sleep Out	Yes																					
Sleep Out	Yes																					
Sleep In	Yes																					
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>dbv_reg[15:8]</th> <th>dbv_reg[7:0]</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>8'h00</td> <td>8'h00</td> </tr> <tr> <td>S/W Reset</td> <td>8'h00</td> <td>8'h00</td> </tr> <tr> <td>H/W Reset</td> <td>8'h00</td> <td>8'h00</td> </tr> </tbody> </table>										Status	dbv_reg[15:8]	dbv_reg[7:0]	Power On Sequence	8'h00	8'h00	S/W Reset	8'h00	8'h00	H/W Reset	8'h00	8'h00
Status	dbv_reg[15:8]	dbv_reg[7:0]																				
Power On Sequence	8'h00	8'h00																				
S/W Reset	8'h00	8'h00																				
H/W Reset	8'h00	8'h00																				

5.2.29. Read Display Brightness Value(52h)

52H		RDDISBV(Read Display Brightness Value)																
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	Default								
Command	Write	0	1	0	1	0	0	1	0	52H								
Parameter	Read	dbv[7:0]								00H								
Description	<p>This command is used to return the brightness value of the display.                      dbv[7:0] is reset when display is in Sleep in mode.                      dbv[7:0] is '0' when bit bctrl of "Write CTRL Display(53h)" command is "0".                      dbv[7:0] is manual set brightness specified with "Write CTRL Display(53h)" command when bctrl bit is '1'.                      When bit bctrl of "Write CTRL Display(53h)" command is '1' or write SLPIN(10h) command, dbv[7:0] output is the brightness value specified with "Write Display Brightness(51h)" command.</p>																	
Restriction	-																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On,Sleep Out	Yes	Sleep Out	Yes	Sleep In	Yes
Status	Availability																	
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Sleep Out	Yes																	
Sleep In	Yes																	
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Status	Default Value																	
Power On Sequence	8'h00																	
S/W Reset	8'h00																	
H/W Reset	8'h00																	

5.2.30. Write CTRL Display Value(53H)

53H		WRCTRLD(Write CTRL Display)																										
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	Default																		
Command	Write	0	1	0	1	0	0	1	1	53H																		
Parameter	Write	sam_ou tdoor3	0	bctrl	0	disp_di m	backlig ht_on	0	0	00H																		
Description	<p>This command is used to control display brightness.                      sam_outdoor3:SAMSUNG outdoor mode enable switch. “1”=open. “0”=close.                      bctrl:Brightness Control Black On/Off. This bit is always used to switch brightness for display.</p> <table border="1"> <thead> <tr> <th>bctrl</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Brightness Control Black Off(dbv[7:0]=00h)</td> </tr> <tr> <td>1</td> <td>Brightness Control Black On(dbv[7:0] is active)</td> </tr> </tbody> </table> <p>disp_dim:Display Dimming Control. This function is only for manual brightness setting.</p> <table border="1"> <thead> <tr> <th>disp_dim</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Display Dimming Off.</td> </tr> <tr> <td>1</td> <td>Display Dimming On.</td> </tr> </tbody> </table> <p>backlight_on:Backlight Control On/Off.</p> <table border="1"> <thead> <tr> <th>backlight_on</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Backlight Control Off.</td> </tr> <tr> <td>1</td> <td>Backlight Control On.</td> </tr> </tbody> </table> <p>Dimming function is adapted to the brightness registers for display when bit bctrl is changed at disp_dim =1,e.g.bctrl:0→1 or 1 → 0.                      When backlight_on bit change from “On” to “Off”,backlight is turned off without gradual dimming,even if Display Dimming On(disp_dim=1) are selected.</p>										bctrl	Description	0	Brightness Control Black Off(dbv[7:0]=00h)	1	Brightness Control Black On(dbv[7:0] is active)	disp_dim	Description	0	Display Dimming Off.	1	Display Dimming On.	backlight_on	Description	0	Backlight Control Off.	1	Backlight Control On.
	bctrl	Description																										
0	Brightness Control Black Off(dbv[7:0]=00h)																											
1	Brightness Control Black On(dbv[7:0] is active)																											
disp_dim	Description																											
0	Display Dimming Off.																											
1	Display Dimming On.																											
backlight_on	Description																											
0	Backlight Control Off.																											
1	Backlight Control On.																											
Restriction	-																											
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	Status	Availability																										
	Normal Mode On,Sleep Out	Yes																										
	Sleep Out	Yes																										
Sleep In	Yes																											

Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>8'h00</td> </tr> <tr> <td>S/W Reset</td> <td>8'h00</td> </tr> <tr> <td>H/W Reset</td> <td>8'h00</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	8'h00	S/W Reset	8'h00	H/W Reset	8'h00
	Status	Default Value								
	Power On Sequence	8'h00								
	S/W Reset	8'h00								
H/W Reset	8'h00									

### 5.2.31. Read CTRL Display Value(54H)

54H		RDCTRLD(Read CTRL Display Value)																
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	Default								
Command	Write	0	1	0	1	0	1	0	0	54H								
Parameter	Read	0	0	bctrl	0	disp_dim	backlight_on	0	0	00H								
Description	This command is used to read the control status of display brightness. bctrl: display brightness control. backlight_on: backlight control. disp_dim: display dimming control.																	
Restriction	-																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On,Sleep Out	Yes	Sleep Out	Yes	Sleep In	Yes
Status	Availability																	
Normal Mode On,Sleep Out	Yes																	
Sleep Out	Yes																	
Sleep In	Yes																	
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>8'h00</td> </tr> <tr> <td>S/W Reset</td> <td>8'h00</td> </tr> <tr> <td>H/W Reset</td> <td>8'h00</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	8'h00	S/W Reset	8'h00	H/W Reset	8'h00
Status	Default Value																	
Power On Sequence	8'h00																	
S/W Reset	8'h00																	
H/W Reset	8'h00																	

5.2.32. Read Display ID1(DAH)

DAH	RDID1(Read Display ID1)																		
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	Default									
Command	Write	1	1	0	1	1	0	1	0	DAH									
Parameter	Read	id1								30h									
Description	<p>This read byte is used to track the LCD module/driver version. It is defined by the display supplier (with User's agreement) and changes each time a revision is made to the display, material or construction specifications.</p> <p>The parameter is LCD module's manufacturer ID.</p> <p>The id1 is programmed by OTP function.</p>																		
Restriction	-																		
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On,Sleep Out	Yes	Sleep Out	Yes	Sleep In	Yes	
Status	Availability																		
Normal Mode On,Sleep Out	Yes																		
Sleep Out	Yes																		
Sleep In	Yes																		
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value (Before OTP program)</th> <th>Default Value (Before OTP program)</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>8'h30</td> <td>OTP value</td> </tr> <tr> <td>H/W Reset</td> <td>8'h30</td> <td>OTP value</td> </tr> </tbody> </table>										Status	Default Value (Before OTP program)	Default Value (Before OTP program)	Power On Sequence	8'h30	OTP value	H/W Reset	8'h30	OTP value
Status	Default Value (Before OTP program)	Default Value (Before OTP program)																	
Power On Sequence	8'h30	OTP value																	
H/W Reset	8'h30	OTP value																	



5.2.33. Read Display ID2(DBH)

DBH		RDID2(Read Display ID2)																	
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	Default									
Command	Write	1	1	0	1	1	0	1	1	DBH									
Parameter	Read	id2								52h									
Description	This read byte is used to track the LCD module/driver version. It is defined by the display supplier (with User's agreement) and changes each time a revision is made to the display, material or construction specifications. The parameter is LCD module/driver version ID. The id2 is programmed by OTP function.																		
Restriction	-																		
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On,Sleep Out	Yes	Sleep Out	Yes	Sleep In	Yes	
Status	Availability																		
Normal Mode On,Sleep Out	Yes																		
Sleep Out	Yes																		
Sleep In	Yes																		
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value (Before OTP program)</th> <th>Default Value (Before OTP program)</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>8'h52</td> <td>OTP value</td> </tr> <tr> <td>H/W Reset</td> <td>8'h52</td> <td>OTP value</td> </tr> </tbody> </table>										Status	Default Value (Before OTP program)	Default Value (Before OTP program)	Power On Sequence	8'h52	OTP value	H/W Reset	8'h52	OTP value
Status	Default Value (Before OTP program)	Default Value (Before OTP program)																	
Power On Sequence	8'h52	OTP value																	
H/W Reset	8'h52	OTP value																	

5.2.34. Read Display ID3(DCH)

DCH		RDID3(Read ID3)																	
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	Default									
Command	Write	1	1	0	1	1	1	0	0	DCH									
Parameter	Read	id3								01H									
Description	<p>This read byte is used to track the LCD module/driver version. It is defined by the display supplier (with User's agreement) and changes each time a revision is made to the display, material or construction specifications.</p> <p>The parameter is LCD module/driver version ID.</p> <p>The id3 is programmed by OTP function.</p>																		
Restriction	-																		
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On,Sleep Out	Yes	Sleep Out	Yes	Sleep In	Yes	
Status	Availability																		
Normal Mode On,Sleep Out	Yes																		
Sleep Out	Yes																		
Sleep In	Yes																		
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value (Before OTP program)</th> <th>Default Value (Before OTP program)</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>8'h01</td> <td>OTP value</td> </tr> <tr> <td>H/W Reset</td> <td>8'h01</td> <td>OTP value</td> </tr> </tbody> </table>										Status	Default Value (Before OTP program)	Default Value (Before OTP program)	Power On Sequence	8'h01	OTP value	H/W Reset	8'h01	OTP value
Status	Default Value (Before OTP program)	Default Value (Before OTP program)																	
Power On Sequence	8'h01	OTP value																	
H/W Reset	8'h01	OTP value																	

5.2.35. EXTC Command Set enable register (FFH)

FFh		ENEXTC (EXTC Command Set Enable Register)																	
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	Default									
Command	Write	1	1	1	1	1	1	1	1	FFH									
Parameter	Write	0	0	0	0	0	0	page[1:0]		00H									
Description	Config page. Write three times. The first time write 30h, the second time write 52h, the last time write page[1:0].																		
		<table border="1"> <thead> <tr> <th>page</th> <th>Descriptions</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>select page0</td> </tr> <tr> <td>01</td> <td>select page1</td> </tr> <tr> <td>10</td> <td>select page2</td> </tr> </tbody> </table>		page	Descriptions	00	select page0	01	select page1	10	select page2								
page	Descriptions																		
00	select page0																		
01	select page1																		
10	select page2																		
Restriction	-																		
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On,Sleep Out	Yes	Sleep Out	Yes	Sleep In	Yes	
Status	Availability																		
Normal Mode On,Sleep Out	Yes																		
Sleep Out	Yes																		
Sleep In	Yes																		
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>8'h00</td> </tr> <tr> <td>S/W Reset</td> <td>8'h00</td> </tr> <tr> <td>H/W Reset</td> <td>8'h00</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	8'h00	S/W Reset	8'h00	H/W Reset	8'h00	
Status	Default Value																		
Power On Sequence	8'h00																		
S/W Reset	8'h00																		
H/W Reset	8'h00																		

Customer Command List

Page 1 command													
Instruction	DCX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
IFCTRL2	0	↑	1	0	0	1	0	0	0	0	1	21h	interface_ctrl
	1	↑	1	0	0	0	0	pad_sel	1	0	0	04h	-
VCOM_ADJ1	0	↑	1	0	0	1	1	0	1	1	1	37h	vcom_adj
	1	↑	1	vap_adj								dch	-
VCOM_ADJ2	0	↑	1	0	0	1	1	1	0	0	0	38h	vcom_adj
	1	↑	1	van_adj								57h	-
VCOM_ADJ3	1	↑	1	0	0	1	1	1	0	0	1	39h	vcom_adj
	1	↑	1	vcom_adj								41h	-
VCOM_ADJ4	0	↑	1	0	0	1	1	1	0	1	0	3Ah	vcom_adj
	1	↑	1	vcom2_adj								20h	-
PADCTRL1	0	↑	1	0	1	0	0	1	0	0	0	48h	pad_ctrl
	1	↑	1	0	0	vcom_hiz	0	sdo_oe	ledpw_m_oe	te_oe	te1_oe	0fh	-
BOOST_CTRL1	0	↑	1	1	0	0	0	0	0	0	0	80h	pump_ctrl
	1	↑	1	0	0	boostm[1:0]		0	0	0	0	10h	-
BOOST_CTRL2	0	↑	1	1	0	0	0	0	0	0	1	81h	pump_ctrl
	1	↑	1	0	0	drvn[1:0]		0	0	drvp[1:0]		11h	-
EXTPW_CTRL1	0	↑	1	1	0	0	1	0	0	0	0	90h	pump_ctrl
	1	↑	1	1	1	1	0	ext_dm_nor[1:0]		ext_dm_pwr[1:0]		E5h	-
EXTPW_CTRL2	0	↑	1	1	0	0	1	0	0	0	1	91h	pump_ctrl
	1	↑	1	0	ext_clkp_nor_width[2:0]			0	ext_clkp_pwr_width[2:0]			44h	-
EXTPW_CTRL3	0	↑	1	1	0	0	1	0	0	1	0	92h	pump_ctrl
	1	↑	1	0	ext_clkn_nor_width[2:0]			0	ext_clkn_pwr_width[2:0]			44h	-
PUMP_CTRL1	0	↑	1	1	0	0	1	1	0	0	0	98h	pump_ctrl
	1	↑	1	vgh_cm_p_en	vgh_amp_en	vgh_sync	0	pump_ss_width[1:0]		vgh_sel[1:0]		4ah	-
PUMP_CTRL2	0	↑	1	1	0	0	1	1	0	0	1	99h	pump_ctrl
	1	↑	1	vgh_clk_sel[3:0]				vgh_clamp[3:0]				54h	-
PUMP_CTRL3	0	↑	1	1	0	0	1	1	0	1	0	9Ah	pump_ctrl
	1	↑	1	vgl_cmp_en	vgl_amp_en	vgl_sync	0	0	0	vgl_sel[1:0]		41h	-
PUMP_CTRL4	0	↑	1	1	0	0	1	1	0	1	1	9Bh	pump_ctrl
	1	↑	1	vgl_clk_sel[3:0]				vgl_clamp[3:0]				56h	-

Page 1 command													
Instruction	DCX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
LVDS_CTRL1	0	↑	1	1	1	1	0	0	0	0	0	D0h	lvds_ctrl
	1	↑	1	0	0	0	0	0	lvfmt	lvbit	lvds_en	06h	-
LVDS_CTRL8	0	↑	1	1	1	1	0	0	1	1	1	D7h	lvds_ctrl
	1	↑	1	0	pol_swap	0	0	lane_swap[3:0]			00h	-	
ENEXTC	0	↑	1	1	1	1	1	1	1	1	1	FFh	EXTC Command Set Enable Register
	1	↑	1	0	0	0	0	0	0	page[1:0]		00h	-

### 5.3. Customer Command List and Description

#### 5.3.1. IFCTRL2: 21H

Address	IFCTRL2								
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
21H	0	0	0	0	pad_sel	1	0	0	04H

pad\_sel: 0:SPI send "1129" to make the chip enter display on mode,1:pad(RS1) rising edge to make the chip enter display on mode.

5.3.2. vcom\_adj:37H~3AH

Address	vcom_adj									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default	
37h	vap_adj								dcH	
38h	van_adj								57H	
39h	vcom_adj								41H	
3Ah	vcom2_adj								20H	
Description	vap_adj: Set the output voltage for VGMP.									
	vap_adj[7:0] (Hex)	VGMP (V)	vap_adj[7:0] (Hex)	VGMP (V)	vap_adj[7:0] (Hex)	VGMP (V)	vap_adj[7:0] (Hex)	VGMP (V)		
	00H	2.64	10H	2.842	20H	3.043	30H	3.244		
	01H	2.653	11H	2.854	21H	3.055	31H	3.257		
	02H	2.666	12H	2.867	22H	3.068	32H	3.269		
	03H	2.678	13H	2.879	23H	3.08	33H	3.282		
	04H	2.691	14H	2.892	24H	3.093	34H	3.294		
	05H	2.703	15H	2.904	25H	3.106	35H	3.307		
	06H	2.716	16H	2.917	26H	3.118	36H	3.319		
	07H	2.728	17H	2.93	27H	3.131	37H	3.332		
	08H	2.741	18H	2.942	28H	3.143	38H	3.345		
	09H	2.754	19H	2.955	29H	3.156	39H	3.357		
	0AH	2.766	1AH	2.967	2AH	3.168	3AH	3.37		
	0BH	2.779	1BH	2.98	2BH	3.181	3BH	3.382		
	0CH	2.791	1CH	2.992	2CH	3.194	3CH	3.395		
	0DH	2.804	1DH	3.005	2DH	3.206	3DH	3.407		
	0EH	2.816	1EH	3.018	2EH	3.219	3EH	3.42		
	0FH	2.829	1FH	3.03	2FH	3.231	3FH	3.433		
		vap_adj[7:0] (Hex)	VGMP (V)	vap_adj[7:0] (Hex)	VGMP (V)	vap_adj[7:0] (Hex)	VGMP (V)	vap_adj[7:0] (Hex)	VGMP (V)	
		40H	3.445	50H	3.646	60H	3.848	70H	4.049	
		41H	3.458	51H	3.659	61H	3.86	71H	4.062	
		42H	3.47	52H	3.672	62H	3.873	72H	4.075	
		43H	3.483	53H	3.684	63H	3.886	73H	4.087	
		44H	3.495	54H	3.697	64H	3.898	74H	4.1	
		45H	3.508	55H	3.709	65H	3.911	75H	4.112	
		46H	3.521	56H	3.722	66H	3.923	76H	4.125	
		47H	3.533	57H	3.735	67H	3.936	77H	4.138	
		48H	3.546	58H	3.747	68H	3.949	78H	4.15	
	49H	3.558	59H	3.76	69H	3.961	79H	4.163		
	4AH	3.571	5AH	3.772	6AH	3.974	7AH	4.176		
	4BH	3.584	5BH	3.785	6BH	3.986	7BH	4.188		
	4CH	3.596	5CH	3.797	6CH	3.999	7CH	4.201		
	4DH	3.609	5DH	3.81	6DH	4.012	7DH	4.213		
	4EH	3.621	5EH	3.823	6EH	4.024	7EH	4.226		
	4FH	3.634	5FH	3.835	6FH	4.037	7FH	4.239		

vap_adj[7:0] (Hex)	VGMP (V)	vap_adj[7:0] (Hex)	VGMP (V)	vap_adj[7:0] (Hex)	VGMP (V)	vap_adj[7:0] (Hex)	VGMP (V)
80H	4.251	90H	4.454	A0H	4.655	B0H	4.856
81H	4.264	91H	4.466	A1H	4.668	B1H	4.868
82H	4.277	92H	4.479	A2H	4.68	B2H	4.881
83H	4.289	93H	4.492	A3H	4.693	B3H	4.894
84H	4.302	94H	4.504	A4H	4.705	B4H	4.906
85H	4.314	95H	4.517	A5H	4.718	B5H	4.919
86H	4.327	96H	4.529	A6H	4.73	B6H	4.931
87H	4.34	97H	4.542	A7H	4.743	B7H	4.944
88H	4.352	98H	4.555	A8H	4.756	B8H	4.956
89H	4.365	99H	4.567	A9H	4.768	B9H	4.969
8AH	4.378	9AH	4.58	AAH	4.781	BAH	4.981
8BH	4.39	9BH	4.592	ABH	4.793	BBH	4.994
8CH	4.403	9CH	4.605	ACH	4.806	BCH	5.006
8DH	4.416	9DH	4.618	ADH	4.818	BDH	5.019
8EH	4.428	9EH	4.63	AEH	4.831	BEH	5.031
8FH	4.441	9FH	4.643	AFH	4.843	BFH	5.044

vap_adj[7:0] (Hex)	VGMP (V)	vap_adj[7:0] (Hex)	VGMP (V)	vap_adj[7:0] (Hex)	VGMP (V)	vap_adj[7:0] (Hex)	VGMP (V)
C0H	5.057	D0H	5.257	E0H	5.458	F0H	5.659
C1H	5.069	D1H	5.27	E1H	5.471	F1H	5.671
C2H	5.082	D2H	5.282	E2H	5.483	F2H	5.684
C3H	5.094	D3H	5.295	E3H	5.496	F3H	5.696
C4H	5.107	D4H	5.307	E4H	5.508	F4H	5.709
C5H	5.119	D5H	5.32	E5H	5.521	F5H	5.721
C6H	5.132	D6H	5.333	E6H	5.533	F6H	5.734
C7H	5.144	D7H	5.345	E7H	5.546	F7H	5.746
C8H	5.157	D8H	5.358	E8H	5.558	F8H	5.759
C9H	5.169	D9H	5.37	E9H	5.571	F9H	5.771
CAH	5.182	DAH	5.383	EAH	5.583	FAH	5.784
CBH	5.195	DBH	5.395	EBH	5.596	FBH	5.796
CCH	5.207	DCH	5.408	ECH	5.609	FCH	5.809
CDH	5.22	DDH	5.42	EDH	5.621	FDH	5.821
CEH	5.232	DEH	5.433	EEH	5.634	FEH	5.834
CFH	5.245	DFH	5.445	EFH	5.646	FFH	5.846

van\_adj: Set the output voltage for VG MN.

van_adj[7:0] (Hex)	VG MN (V)	van_adj[7:0] (Hex)	VG MN (V)	van_adj[7:0] (Hex)	VG MN (V)	van_adj[7:0] (Hex)	VG MN (V)
00H	-2.509	10H	-2.709	20H	-2.91	30H	-3.11
01H	-2.522	11H	-2.722	21H	-2.922	31H	-3.122
02H	-2.534	12H	-2.734	22H	-2.935	32H	-3.135
03H	-2.547	13H	-2.747	23H	-2.947	33H	-3.147
04H	-2.559	14H	-2.759	24H	-2.96	34H	-3.16
05H	-2.572	15H	-2.772	25H	-2.972	35H	-3.173
06H	-2.584	16H	-2.784	26H	-2.985	36H	-3.185
07H	-2.597	17H	-2.797	27H	-2.997	37H	-3.198
08H	-2.609	18H	-2.81	28H	-3.01	38H	-3.21



09H	-2.622	19H	-2.822	29H	-3.022	39H	-3.223
0AH	-2.634	1AH	-2.835	2AH	-3.035	3AH	-3.235
0BH	-2.647	1BH	-2.847	2BH	-3.047	3BH	-3.248
0CH	-2.659	1CH	-2.86	2CH	-3.06	3CH	-3.26
0DH	-2.672	1DH	-2.872	2DH	-3.072	3DH	-3.273
0EH	-2.684	1EH	-2.885	2EH	-3.085	3EH	-3.285
0FH	-2.697	1FH	-2.897	2FH	-3.097	3FH	-3.298

van_adj[7:0] (Hex)	VGMN (V)	van_adj[7:0] (Hex)	VGMN (V)	van_adj[7:0] (Hex)	VGMN (V)	van_adj[7:0] (Hex)	VGMN (V)
40H	-3.31	50H	-3.511	60H	-3.711	70H	-3.911
41H	-3.323	51H	-3.523	61H	-3.724	71H	-3.924
42H	-3.335	52H	-3.536	62H	-3.736	72H	-3.936
43H	-3.348	53H	-3.548	63H	-3.749	73H	-3.949
44H	-3.36	54H	-3.561	64H	-3.761	74H	-3.962
45H	-3.373	55H	-3.573	65H	-3.774	75H	-3.974
46H	-3.385	56H	-3.586	66H	-3.786	76H	-3.987
47H	-3.398	57H	-3.598	67H	-3.799	77H	-3.999
48H	-3.41	58H	-3.611	68H	-3.811	78H	-4.012
49H	-3.423	59H	-3.623	69H	-3.824	79H	-4.024
4AH	-3.435	5AH	-3.636	6AH	-3.836	7AH	-4.037
4BH	-3.448	5BH	-3.648	6BH	-3.849	7BH	-4.049
4CH	-3.461	5CH	-3.661	6CH	-3.861	7CH	-4.062
4DH	-3.473	5DH	-3.673	6DH	-3.874	7DH	-4.074
4EH	-3.486	5EH	-3.686	6EH	-3.886	7EH	-4.087
4FH	-3.498	5FH	-3.698	6FH	-3.899	7FH	-4.099

van_adj[7:0] (Hex)	VGMN (V)	van_adj[7:0] (Hex)	VGMN (V)	van_adj[7:0] (Hex)	VGMN (V)	van_adj[7:0] (Hex)	VGMN (V)
80H	-4.112	90H	-4.312	A0H	-4.513	B0H	-4.713
81H	-4.124	91H	-4.325	A1H	-4.525	B1H	-4.726
82H	-4.137	92H	-4.337	A2H	-4.538	B2H	-4.738
83H	-4.149	93H	-4.35	A3H	-4.55	B3H	-4.751
84H	-4.162	94H	-4.362	A4H	-4.563	B4H	-4.763
85H	-4.174	95H	-4.375	A5H	-4.575	B5H	-4.776
86H	-4.187	96H	-4.387	A6H	-4.588	B6H	-4.788
87H	-4.2	97H	-4.4	A7H	-4.6	B7H	-4.801
88H	-4.212	98H	-4.412	A8H	-4.613	B8H	-4.813
89H	-4.225	99H	-4.425	A9H	-4.625	B9H	-4.826
8AH	-4.237	9AH	-4.438	AAH	-4.638	BAH	-4.838
8BH	-4.25	9BH	-4.45	ABH	-4.65	BBH	-4.851
8CH	-4.262	9CH	-4.463	ACH	-4.663	BCH	-4.863
8DH	-4.275	9DH	-4.475	ADH	-4.676	BDH	-4.876
8EH	-4.287	9EH	-4.488	AEH	-4.688	BEH	-4.888
8FH	-4.3	9FH	-4.5	AFH	-4.701	BFH	-4.901

van_adj[7:0] (Hex)	VGMN (V)	van_adj[7:0] (Hex)	VGMN (V)	van_adj[7:0] (Hex)	VGMN (V)	van_adj[7:0] (Hex)	VGMN (V)
C0H	-4.913	D0H	-5.114	E0H	-5.314	F0H	-5.515
C1H	-4.926	D1H	-5.126	E1H	-5.327	F1H	-5.527

C2H	-4.939	D2H	-5.139	E2H	-5.339	F2H	-5.54
C3H	-4.951	D3H	-5.151	E3H	-5.352	F3H	-5.552
C4H	-4.964	D4H	-5.164	E4H	-5.364	F4H	-5.565
C5H	-4.976	D5H	-5.177	E5H	-5.377	F5H	-5.577
C6H	-4.989	D6H	-5.189	E6H	-5.389	F6H	-5.59
C7H	-5.001	D7H	-5.202	E7H	-5.402	F7H	-5.602
C8H	-5.014	D8H	-5.214	E8H	-5.414	F8H	-5.615
C9H	-5.026	D9H	-5.227	E9H	-5.427	F9H	-5.627
CAH	-5.039	DAH	-5.239	EAH	-5.44	FAH	-5.64
CBH	-5.051	DBH	-5.252	EBH	-5.452	FBH	-5.652
CCH	-5.064	DCH	-5.264	ECH	-5.465	FCH	-5.665
CDH	-5.076	DDH	-5.277	EDH	-5.477	FDH	-5.677
CEH	-5.089	DEH	-5.289	EEH	-5.49	FEH	-5.69
CFH	-5.101	DFH	-5.302	EFH	-5.502	FFH	-5.702

vcom\_adj: Set the output voltage for VCOM.

vcom_adj[7:0] (Hex)	VCOM (V)	vcom_adj[7:0] (Hex)	VCOM (V)	vcom_adj[7:0] (Hex)	VCOM (V)	vcom_adj[7:0] (Hex)	VCOM (V)
00H	0.0000	10H	-0.3875	20H	-0.5875	30H	-0.7875
01H	-0.2000	11H	-0.4000	21H	-0.6000	31H	-0.8000
02H	-0.2125	12H	-0.4125	22H	-0.6125	32H	-0.8125
03H	-0.2250	13H	-0.4250	23H	-0.6250	33H	-0.8250
04H	-0.2375	14H	-0.4375	24H	-0.6375	34H	-0.8375
05H	-0.2500	15H	-0.4500	25H	-0.6500	35H	-0.8500
06H	-0.2625	16H	-0.4625	26H	-0.6625	36H	-0.8625
07H	-0.2750	17H	-0.4750	27H	-0.6750	37H	-0.8750
08H	-0.2875	18H	-0.4875	28H	-0.6875	38H	-0.8875
09H	-0.3000	19H	-0.5000	29H	-0.7000	39H	-0.9000
0AH	-0.3125	1AH	-0.5125	2AH	-0.7125	3AH	-0.9125
0BH	-0.3250	1BH	-0.5250	2BH	-0.7250	3BH	-0.9250
0CH	-0.3375	1CH	-0.5375	2CH	-0.7375	3CH	-0.9375
0DH	-0.3500	1DH	-0.5500	2DH	-0.7500	3DH	-0.9500
0EH	-0.3625	1EH	-0.5625	2EH	-0.7625	3EH	-0.9625
0FH	-0.3750	1FH	-0.5750	2FH	-0.7750	3FH	-0.9750

vcom_adj[7:0] (Hex)	VCOM (V)	vcom_adj[7:0] (Hex)	VCOM (V)	vcom_adj[7:0] (Hex)	VCOM (V)	vcom_adj[7:0] (Hex)	VCOM (V)
40H	-0.9875	50H	-1.1875	60H	-1.3875	70H	-1.5875
41H	-1.0000	51H	-1.2000	61H	-1.4000	71H	-1.6000
42H	-1.0125	52H	-1.2125	62H	-1.4125	72H	-1.6125
43H	-1.0250	53H	-1.2250	63H	-1.4250	73H	-1.6250
44H	-1.0375	54H	-1.2375	64H	-1.4375	74H	-1.6375
45H	-1.0500	55H	-1.2500	65H	-1.4500	75H	-1.6500
46H	-1.0625	56H	-1.2625	66H	-1.4625	76H	-1.6625
47H	-1.0750	57H	-1.2750	67H	-1.4750	77H	-1.6750
48H	-1.0875	58H	-1.2875	68H	-1.4875	78H	-1.6875
49H	-1.1000	59H	-1.3000	69H	-1.5000	79H	-1.7000
4AH	-1.1125	5AH	-1.3125	6AH	-1.5125	7AH	-1.7125
4BH	-1.1250	5BH	-1.3250	6BH	-1.5250	7BH	-1.7250
4CH	-1.1375	5CH	-1.3375	6CH	-1.5375	7CH	-1.7375
4DH	-1.1500	5DH	-1.3500	6DH	-1.5500	7DH	-1.7500
4EH	-1.1625	5EH	-1.3625	6EH	-1.5625	7EH	-1.7625

4FH	-1.1750	5FH	-1.3750	6FH	-1.5750	7FH	-1.7750
vcom_adj[7:0] (Hex)	VCOM (V)	vcom_adj[7:0] (Hex)	VCOM (V)	vcom_adj[7:0] (Hex)	VCOM (V)	vcom_adj[7:0] (Hex)	VCOM (V)
80H	-1.7875	90H	-1.9875	A0H	-2.1875	B0H	-2.3875
81H	-1.8000	91H	-2.0000	A1H	-2.2000	B1H	-2.4000
82H	-1.8125	92H	-2.0125	A2H	-2.2125	B2H	-2.4125
83H	-1.8250	93H	-2.0250	A3H	-2.2250	B3H	-2.4250
84H	-1.8375	94H	-2.0375	A4H	-2.2375	B4H	-2.4375
85H	-1.8500	95H	-2.0500	A5H	-2.2500	B5H	-2.4500
86H	-1.8625	96H	-2.0625	A6H	-2.2625	B6H	-2.4625
87H	-1.8750	97H	-2.0750	A7H	-2.2750	B7H	-2.4750
88H	-1.8875	98H	-2.0875	A8H	-2.2875	B8H	-2.4875
89H	-1.9000	99H	-2.1000	A9H	-2.3000	B9H	-2.5000
8AH	-1.9125	9AH	-2.1125	AAH	-2.3125	BAH	-2.5125
8BH	-1.9250	9BH	-2.1250	ABH	-2.3250	BBH	-2.5250
8CH	-1.9375	9CH	-2.1375	ACH	-2.3375	BCH	-2.5375
8DH	-1.9500	9DH	-2.1500	ADH	-2.3500	BDH	-2.5500
8EH	-1.9625	9EH	-2.1625	AEH	-2.3625	BEH	-2.5625
8FH	-1.9750	9FH	-2.1750	AFH	-2.3750	BFH	-2.5750

vcom_adj[7:0] (Hex)	VCOM (V)	vcom_adj[7:0] (Hex)	VCOM (V)	vcom_adj[7:0] (Hex)	VCOM (V)	vcom_adj[7:0] (Hex)	VCOM (V)
C0H	-2.5875	D0H	-2.7875	E0H	-2.9875	F0H	-3.1875
C1H	-2.6000	D1H	-2.8000	E1H	-3.0000	F1H	-3.2000
C2H	-2.6125	D2H	-2.8125	E2H	-3.0125	F2H	-3.2125
C3H	-2.6250	D3H	-2.8250	E3H	-3.0250	F3H	-3.2250
C4H	-2.6375	D4H	-2.8375	E4H	-3.0375	F4H	-3.2375
C5H	-2.6500	D5H	-2.8500	E5H	-3.0500	F5H	-3.2500
C6H	-2.6625	D6H	-2.8625	E6H	-3.0625	F6H	-3.2625
C7H	-2.6750	D7H	-2.8750	E7H	-3.0750	F7H	-3.2750
C8H	-2.6875	D8H	-2.8875	E8H	-3.0875	F8H	-3.2875
C9H	-2.7000	D9H	-2.9000	E9H	-3.1000	F9H	-3.3000
CAH	-2.7125	DAH	-2.9125	EAH	-3.1125	FAH	-3.3125
CBH	-2.7250	DBH	-2.9250	EBH	-3.1250	FBH	-3.3250
CCH	-2.7375	DCH	-2.9375	ECH	-3.1375	FCH	-3.3375
CDH	-2.7500	DDH	-2.9500	EDH	-3.1500	FDH	-3.3500
CEH	-2.7625	DEH	-2.9625	EEH	-3.1625	FEH	-3.3625
CFH	-2.7750	DFH	-2.9750	EFH	-3.1750	FFH	-3.3750

vcom2\_adj: Set the output voltage for VCOM when power down.

5.3.3. PADCTRL1: 48H

Address	PADCTRL1								
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
48H	0	0	vcom_hiz	0	sdo_oe	ledpwm_oe	te_oe	te1_oe	0fH
vcom_hiz : Set VCOM Hi-Z state when disable.H: enable;L: disable. sdo_oe : sdo output enable.0: Hi-Z;1:output. te1_oe : te1 pad outout enable.0: Hi-Z;1: output. te_oe : te pad outout enable.0:Hi-Z;1: output. ledpwm_oe : ledpwm pad outout enable.0: Hi-Z;1:output.									

5.3.4. BOOST\_CTRL1~2 : 80h~81h

Address	BOOST_CTRL1~2																	
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default									
80h	0	0	boostm[1:0]		0	0	0	0	10H									
81h	0	0	drvn[1:0]		0	0	drvp[1:0]		11H									
Description	boostm[1:0]: It is used to select power mode.																	
	<table border="1"> <thead> <tr> <th>BOOSTM[1]</th> <th>BOOSTM[0]</th> <th>Mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1</td> <td>Mode-8, External VSP and VSN</td> </tr> <tr> <td>1</td> <td>0</td> <td>Mode-3, Power IC</td> </tr> </tbody> </table>									BOOSTM[1]	BOOSTM[0]	Mode	0	1	Mode-8, External VSP and VSN	1	0	Mode-3, Power IC
	BOOSTM[1]	BOOSTM[0]	Mode															
	0	1	Mode-8, External VSP and VSN															
	1	0	Mode-3, Power IC															
drvn[1:0] : Driving capacity of DC2DCN driver.																		
<table border="1"> <thead> <tr> <th>DRVN[1:0]</th> <th>Driving Capability of DC2DCN Driver</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>Level 1 (weak)</td> </tr> <tr> <td>01</td> <td>Level 2 (default)</td> </tr> <tr> <td>10</td> <td>Level 3</td> </tr> <tr> <td>11</td> <td>Level 4 (strong)</td> </tr> </tbody> </table>									DRVN[1:0]	Driving Capability of DC2DCN Driver	00	Level 1 (weak)	01	Level 2 (default)	10	Level 3	11	Level 4 (strong)
DRVN[1:0]	Driving Capability of DC2DCN Driver																	
00	Level 1 (weak)																	
01	Level 2 (default)																	
10	Level 3																	
11	Level 4 (strong)																	
drvp[1:0]: Driving capacity of D2DCP driver.																		
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DRVP[1:0]	Driving Capability of DC2DCP Driver																	
00	Level 1 (weak)																	
01	Level 2 (default)																	
10	Level 3																	
11	Level 4 (strong)																	

5.3.5. EXTPW\_CTRL1~3:90H~92H

Address	EXTPW_CTRL1~3																											
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default																			
90H	1	1	1	0	ext_dm_nor[1:0]		ext_dm_pwr[1:0]		e5H																			
91H	0	ext_clkp_nor_width[2:0]			0	ext_clkp_pwr_width[2:0]			44H																			
92H	0	ext_clkn_nor_width[2:0]			0	ext_clkn_pwr_width[2:0]			44H																			
Description	ext_dm_nor[1:0]: External power IC mode Pump ratio setting at normal display.																											
	<table border="1"> <thead> <tr> <th>ext_dm_nor[1:0]</th> <th>VSP pump ratio</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>1.5xVCI</td> </tr> <tr> <td>01</td> <td>2.0xVCI</td> </tr> <tr> <td>10</td> <td>3.0 xVCI</td> </tr> <tr> <td>11</td> <td>3.0 xVCI</td> </tr> </tbody> </table>									ext_dm_nor[1:0]	VSP pump ratio	00	1.5xVCI	01	2.0xVCI	10	3.0 xVCI	11	3.0 xVCI									
	ext_dm_nor[1:0]	VSP pump ratio																										
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ext_clkp_nor_width[2:0]	CLK Frequency	ext_clkp_nor_width[2:0]	CLK Frequency																									
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ext_clkn_nor_width[2:0]: External Power IC clkn ratio setting when normal display.																												
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000	1/16 times	100	1 times
001	1/8 times	101	2 times
010	1/4 times	110	4 times
011	1/2 times	111	8 times

ext\_clkn\_pwr\_width[2:0]: External Power IC clkn ratio setting when power on region.

ext_clkn_pwr_width[2:0]	CLK Frequency	ext_clkn_pwr_width[2:0]	CLK Frequency
000	1/16 times	100	1 times
001	1/8 times	101	2 times
010	1/4 times	110	4 times
011	1/2 times	111	8 times

5.3.6. PUMP\_CTRL1~4:98H~9BH

Address	PUMP_CTRL1~4								
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
98H	vgh_cmp_en	vgh_amp_en	vgh_sync	0	pump_ss_width[1:0]		vgh_sel[1:0]		4aH
99H	vgh_clk_sel[3:0]				vgh_clamp[3:0]				54H
9AH	vgl_cmp_en	vgl_amp_en	vgl_sync	0	0	0	vgl_sel[1:0]		41H
9BH	vgl_clk_sel[3:0]				vgl_clamp[3:0]				56H
Description	vgh_cmp_en: VGH pump output clamp using digital mode.								
	vgh_cmp_en		VGH clamp digital mode						
	0		Disable						
	1		Enable						
	vgh_amp_en: VGH pump output clamp using linear mode.								
	vgh_amp_en		VGH clamp linear mode						
	0		Disable						
	1		Enable						
	Note: when vgh_amp_en and vgh_cmp_en are both 1, the VGH pump output clamp will use linear mode as the output clamp working mode.								
	vgh_sync: VGH pump output clamp synchronizes with clock when using digital mode.								
vgh_sync		VGH clamp synchronize function							
0		Disable							
1		Enable							
pump_ss_width[1:0]: Set the soft start time for HV pumps. The longer soft start time, the smaller peak current when pumps pump up, but the longer time to pump to the work voltage. Adjust the soft start time take into account the trade-off between the peak current when pump and pump time.									
pump_ss_width[1:0]		Multiple of soft start time to refresh one line time							
00		128 lines							
01		256 lines							
10		512 lines							
11		1024 lines							
vgh_sel[1:0]: set the factor used in the set-up circuits for VGH. Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.									
vgh_sel[1:0]		VGH OUTPUT							
00		2xVSP							
01		3xVSP							
10		4xVSP							



11	reserved
----	----------

Note: When vpp\_src\_sel=1, then the factor will change as follows.

vgh_sel[1:0]	VGH OUTPUT
00	2xVSP
01	3xVSP
10	2xVSP
11	3xVSP

vgh\_clk\_sel[3:0]: Set the VGH pump's working frequency which is the ratio of the main clock.

vgh_clk_sel[3:0]				VGH pump frequency
0	0	0	0	1/2 times
0	0	0	1	1/4 times
0	0	1	0	1/6 times
0	0	1	1	1/8 times
0	1	0	0	1/10 times
0	1	0	1	1/12 times
0	1	1	0	1/14 times
0	1	1	1	1/16 times
1	0	0	0	1/18 times
1	0	0	1	1/20 times
1	0	1	0	1/22 times
1	0	1	1	1/24 times
1	1	0	0	1/26 times
1	1	0	1	1/28 times
1	1	1	0	1/30 times
1	1	1	1	1/32 times

vgh\_clamp[3:0]: Set the VGH pump's clamp level.

vgh_clamp[3:0]				VGH clamp level(V)
0	0	0	0	11.0
0	0	0	1	12.0
0	0	1	0	13.0
0	0	1	1	14.0
0	1	0	0	15.0
0	1	0	1	15.5
0	1	1	0	16.0
0	1	1	1	16.5
1	0	0	0	17.0
1	0	0	1	17.5
1	0	1	0	18.0
1	0	1	1	reserved
1	1	0	0	reserved
1	1	0	1	reserved
1	1	1	0	reserved
1	1	1	1	reserved

Note: When vpp\_src\_sel=1, then the factor will change as follows.

vgh_clamp_sel[3:0]				VGH clamp level(V)
x	0	0	0	7.5
x	0	0	1	8.0
x	0	1	0	8.5
x	0	1	1	9.0
x	1	0	0	9.5

x	1	0	1	10.0
x	1	1	0	10.5
x	1	1	1	11.0

vgl\_cmp\_en: VGL pump output clamp using digital mode.

vgl_cmp_en	VGL clamp digital mode
0	Disable
1	Enable

vgl\_amp\_en: VGL pump output clamp using linear mode.

vgl_amp_en	VGL clamp linear mode
0	Disable
1	Enable

Note: when vgl\_amp\_en and vgl\_cmp\_en are both 1, the VGL pump output clamp will use linear mode as the output clamp working mode.

vgl\_sync: VGL pump output clamp synchronizes with clock when using digital mode.

vgl_sync	VGL clamp synchronize function
0	Disable
1	Enable

vgl\_sel[1:0]: set the factor used in the set-up circuits for VGL.

Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.

vgl_sel[1:0]	VGL OUTPUT
00	2xVSN
01	3xVSN
10	4xVSN
11	4xVSN

vgl\_clk\_sel[3:0]: Set the VGL pump's working frequency which is the ratio of main clock.

vgl_clk_sel[3:0]				VGL pump frequency
0	0	0	0	1/2 times
0	0	0	1	1/4 times
0	0	1	0	1/6 times
0	0	1	1	1/8 times
0	1	0	0	1/10 times
0	1	0	1	1/12 times
0	1	1	0	1/14 times
0	1	1	1	1/16 times
1	0	0	0	1/18 times
1	0	0	1	1/20 times
1	0	1	0	1/22 times
1	0	1	1	1/24 times
1	1	0	0	1/26 times
1	1	0	1	1/28 times
1	1	1	0	1/30 times
1	1	1	1	1/32 times

vgl\_clamp[3:0]: Set the VGL pump's clamp level.

		vgl_clamp[3:0]				VGL clamp level(V)	
		0	0	0	0	-7.0	
		0	0	0	1	-7.5	
		0	0	1	0	-8.0	
		0	0	1	1	-8.5	
		0	1	0	0	-9.0	
		0	1	0	1	-9.5	
		0	1	1	0	-10.0	
		0	1	1	1	-11.0	
		1	0	0	0	-11.5	
		1	0	0	1	-12.0	
		1	0	1	0	-12.5	
		1	0	1	1	-13.0	
		1	1	0	0	-14.0	
		1	1	0	1	-14.5	
		1	1	1	0	-15.0	
		1	1	1	1	-15.5	

5.3.7.LVDS\_CTRL0,LVDS\_CTRL8:D0H,D7H

Address	LVDS_CTRL0,LVDS_CTRL8																																																																																																										
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default																																																																																																		
D0H	0	0	0	0	0	lvfmt	lvbit	lvds_en	06H																																																																																																		
D7H	0	pol_swap	0	0	lane_swap[3:0]				00H																																																																																																		
Description	lvfmt: L:JDEA format H:VESA format. Lvbit: L:6bit,H:8bit. lvds_en: L:lvds interface disable,H:lvds interface enable. pol_swap:polarity selection.(default:1)																																																																																																										
	<table border="1"> <thead> <tr> <th rowspan="2">pol_swap</th> <th colspan="5">LVDS Lane Mapping</th> </tr> <tr> <th>LVDS_D0P/N</th> <th>LVDS_D1P/N</th> <th>LVDS_CLKP/N</th> <th>LVDS_D2P/N</th> <th>LVDS_D3P/N</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>LVDS_D0N/P</td> <td>LVDS_D1N/P</td> <td>LVDS_CLKN/P</td> <td>LVDS_D2N/P</td> <td>LVDS_D3N/P</td> </tr> <tr> <td>1</td> <td>LVDS_D0P/N</td> <td>LVDS_D1P/N</td> <td>LVDS_CLKP/N</td> <td>LVDS_D2P/N</td> <td>LVDS_D3P/N</td> </tr> </tbody> </table>									pol_swap	LVDS Lane Mapping					LVDS_D0P/N	LVDS_D1P/N	LVDS_CLKP/N	LVDS_D2P/N	LVDS_D3P/N	0	LVDS_D0N/P	LVDS_D1N/P	LVDS_CLKN/P	LVDS_D2N/P	LVDS_D3N/P	1	LVDS_D0P/N	LVDS_D1P/N	LVDS_CLKP/N	LVDS_D2P/N	LVDS_D3P/N																																																																											
	pol_swap	LVDS Lane Mapping																																																																																																									
		LVDS_D0P/N	LVDS_D1P/N	LVDS_CLKP/N	LVDS_D2P/N	LVDS_D3P/N																																																																																																					
	0	LVDS_D0N/P	LVDS_D1N/P	LVDS_CLKN/P	LVDS_D2N/P	LVDS_D3N/P																																																																																																					
1	LVDS_D0P/N	LVDS_D1P/N	LVDS_CLKP/N	LVDS_D2P/N	LVDS_D3P/N																																																																																																						
lane_swap[3:0]:lane swap selection.(default:0010)																																																																																																											
<table border="1"> <thead> <tr> <th colspan="4">lane_swap[3:0]</th> <th>LVDS D0</th> <th>LVDS D1</th> <th>LVDS CLK</th> <th>LVDS D2</th> <th>LVDS D3</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>D3</td> <td>D2</td> <td>CLK</td> <td>D1</td> <td>D0</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>D3</td> <td>CLK</td> <td>D2</td> <td>D1</td> <td>D0</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>D0</td> <td>D1</td> <td>CLK</td> <td>D2</td> <td>D3</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>D0</td> <td>D1</td> <td>D2</td> <td>CLK</td> <td>D3</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>CLK</td> <td>D0</td> <td>D1</td> <td>D2</td> <td>D3</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>1</td> <td>CLK</td> <td>D3</td> <td>D2</td> <td>D1</td> <td>D0</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>D3</td> <td>D2</td> <td>D1</td> <td>D0</td> <td>CLK</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>1</td> <td>D0</td> <td>D1</td> <td>D2</td> <td>D3</td> <td>CLK</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>D3</td> <td>D0</td> <td>CLK</td> <td>D1</td> <td>D2</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>D2</td> <td>D1</td> <td>CLK</td> <td>D0</td> <td>D3</td> </tr> </tbody> </table>									lane_swap[3:0]				LVDS D0	LVDS D1	LVDS CLK	LVDS D2	LVDS D3	0	0	0	0	D3	D2	CLK	D1	D0	0	0	0	1	D3	CLK	D2	D1	D0	0	0	1	0	D0	D1	CLK	D2	D3	0	0	1	1	D0	D1	D2	CLK	D3	0	1	0	0	CLK	D0	D1	D2	D3	0	1	0	1	CLK	D3	D2	D1	D0	0	1	1	0	D3	D2	D1	D0	CLK	0	1	1	1	D0	D1	D2	D3	CLK	1	0	0	0	D3	D0	CLK	D1	D2	1	0	0	1	D2	D1	CLK	D0	D3
lane_swap[3:0]				LVDS D0	LVDS D1	LVDS CLK	LVDS D2	LVDS D3																																																																																																			
0	0	0	0	D3	D2	CLK	D1	D0																																																																																																			
0	0	0	1	D3	CLK	D2	D1	D0																																																																																																			
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0	0	1	1	D0	D1	D2	CLK	D3																																																																																																			
0	1	0	0	CLK	D0	D1	D2	D3																																																																																																			
0	1	0	1	CLK	D3	D2	D1	D0																																																																																																			
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1	0	0	0	D3	D0	CLK	D1	D2																																																																																																			
1	0	0	1	D2	D1	CLK	D0	D3																																																																																																			

5.3.8. ENEXTC:FFH

FFh	ENEXTC																
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default								
Command	1	1	1	1	1	1	1	1	FFH								
Parameter	0	0	0	0	0	0	page[1:0]		00H								
Description	<p>Config page. Write three times. The first time write 30h, the second time write 52h, the last time write page[1:0]</p> <table border="1" data-bbox="692 730 1161 900"> <thead> <tr> <th>page</th> <th>Descriptions</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>select page0</td> </tr> <tr> <td>01</td> <td>select page1</td> </tr> <tr> <td>10</td> <td>select page2</td> </tr> </tbody> </table>									page	Descriptions	00	select page0	01	select page1	10	select page2
page	Descriptions																
00	select page0																
01	select page1																
10	select page2																

Page2 command													
Instruction	DCX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
PGAMVR0	0	↑	1	1	0	1	1	0	0	0	0	B0h	gam_config
	1	↑	1	0	0	vrp0[5:0]					02h	-	
PGAMVR1	0	↑	1	1	0	1	1	0	0	0	1	B1h	gam_config
	1	↑	1	0	0	vrp1[5:0]					02h	-	
PGAMVR2	0	↑	1	1	0	1	1	0	0	1	0	B2h	gam_config
	1	↑	1	0	0	vrp2[5:0]					02h	-	
PGAMVR3	0	↑	1	1	0	1	1	0	0	1	1	B3h	gam_config
	1	↑	1	0	0	vrp3[5:0]					11h	-	
PGAMVR4	0	↑	1	1	0	1	1	0	1	0	0	B4h	gam_config
	1	↑	1	0	0	vrp4[5:0]					16h	-	
PGAMVR5	0	↑	1	1	0	1	1	0	1	0	1	B5h	gam_config
	1	↑	1	0	0	vrp5[5:0]					34h	-	
PGAMPR0	0	↑	1	1	0	1	1	0	1	1	0	B6h	gam_config
	1	↑	1	0	prp0[6:0]					15h	-		
PGAMPR1	0	↑	1	1	0	1	1	0	1	1	1	B7h	gam_config
	1	↑	1	0	prp1[6:0]					32h	-		
PGAMPK0	0	↑	1	1	0	1	1	1	0	0	0	B8h	gam_config
	1	↑	1	0	0	0	pkp0[4:0]				11h	-	
PGAMPK1	0	↑	1	1	0	1	1	1	0	0	1	B9h	gam_config
	1	↑	1	0	0	0	pkp1[4:0]				05h	-	
PGAMPK2	0	↑	1	1	0	1	1	1	0	1	0	BAh	gam_config
	1	↑	1	0	0	0	pkp2[4:0]				18h	-	
PGAMPK3	0	↑	1	1	0	1	1	1	0	1	1	BBh	gam_config
	1	↑	1	0	0	0	pkp3[4:0]				18h	-	
PGAMPK4	0	↑	1	1	0	1	1	1	1	0	0	BCh	gam_config
	1	↑	1	0	0	0	pkp4[4:0]				18h	-	
PGAMPK5	0	↑	1	1	0	1	1	1	1	0	1	BDh	gam_config
	1	↑	1	0	0	0	pkp5[4:0]				18h	-	
PGAMPK6	0	↑	1	1	0	1	1	1	1	1	0	BEh	gam_config
	1	↑	1	0	0	0	pkp6[4:0]				1ah	-	
PGAMPK7	0	↑	1	1	0	1	1	1	1	1	1	BFh	gam_config
	1	↑	1	0	0	0	pkp7[4:0]				0fh	-	
PGAMPK8	0	↑	1	1	1	0	0	0	0	0	0	C0h	gam_config
	1	↑	1	0	0	0	pkp8[4:0]				18h	-	

Page2 command													
Instruction	DCX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
PGAMPK9	0	↑	1	1	1	0	0	0	0	0	1	C1h	gam_config
	1	↑	1	0	0	0	pkn9[4:0]				09h	-	
GAMP0	0	↑	1	1	1	0	0	0	0	1	0	C2h	gam_config
	1	↑	1	0	0	0	gamp0[4:0]				00h	-	
NGAMVR0	0	↑	1	1	1	0	1	0	0	0	0	D0h	gam_config
	1	↑	1	0	0	vrn0[5:0]				02h	-		
NGAMVR1	0	↑	1	1	1	0	1	0	0	0	1	D1h	gam_config
	1	↑	1	0	0	vrn1[5:0]				02h	-		
NGAMVR2	0	↑	1	1	1	0	1	0	0	1	0	D2h	gam_config
	1	↑	1	0	0	vrn2[5:0]				02h	-		
NGAMVR3	0	↑	1	1	1	0	1	0	0	1	1	D3h	gam_config
	1	↑	1	0	0	vrn3[5:0]				11h	-		
NGAMVR4	0	↑	1	1	1	0	1	0	1	0	0	D4h	gam_config
	1	↑	1	0	0	vrn4[5:0]				16h	-		
NGAMVR5	0	↑	1	1	1	0	1	0	1	0	1	D5h	gam_config
	1	↑	1	0	0	vrn5[5:0]				34h	-		
NGAMPR0	0	↑	1	1	1	0	1	0	1	1	0	D6h	gam_config
	1	↑	1	0	prn0[6:0]				15h	-			
NGAMPR1	0	↑	1	1	1	0	1	0	1	1	1	D7h	gam_config
	1	↑	1	0	prn1[6:0]				32h	-			
NGAMPK0	0	↑	1	1	1	0	1	1	0	0	0	D8h	gam_config
	1	↑	1	0	0	0	pkn0[4:0]				11h	-	
NGAMPK1	0	↑	1	1	1	0	1	1	0	0	1	D9h	gam_config
	1	↑	1	0	0	0	pkn1[4:0]				05h	-	
NGAMPK2	0	↑	1	1	1	0	1	1	0	1	0	DAh	gam_config
	1	↑	1	0	0	0	pkn2[4:0]				18h	-	
NGAMPK3	0	↑	1	1	1	0	1	1	0	1	1	DBh	gam_config
	1	↑	1	0	0	0	pkn3[4:0]				18h	-	
NGAMPK4	0	↑	1	1	1	0	1	1	1	0	0	DCh	gam_config
	1	↑	1	0	0	0	pkn4[4:0]				18h	-	
NGAMPK5	0	↑	1	1	1	0	1	1	1	0	1	DDh	gam_config
	1	↑	1	0	0	0	pkn5[4:0]				18h	-	

Page2 command													
Instruction	DCX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
NGAMPK6	0	↑	1	1	1	0	1	1	1	1	0	DEh	gam_config
	1	↑	1	0	0	0	pkn6[4:0]				1ah	-	
NGAMPK7	0	↑	1	1	1	0	1	1	1	1	1	DFh	gam_config
	1	↑	1	0	0	0	pkn7[4:0]				0fh	-	
NGAMPK8	0	↑	1	1	1	1	0	0	0	0	0	E0h	gam_config
	1	↑	1	0	0	0	pkn8[4:0]				18h	-	
NGAMPK9	0	↑	1	1	1	1	0	0	0	0	1	E1h	gam_config
	1	↑	1	0	0	0	pkn9[4:0]				09h	-	
GAMN0	0	↑	1	1	1	1	0	0	0	1	0	E2h	gam_config
	1	↑	1	0	0	0	gamn0[4:0]				00h	-	
ENEXTC	0	↑	1	1	1	1	1	1	1	1	1	FFh	page_ctrl
	1	↑	1	0	0	0	0	0	0	page[1:0]		00h	-



5.3.9. PGAMVR0~5;PGAMPR0~1;PGAMPK0~9;GAMP0:B0H~C2H

Address	PGAMVR0~5;PGAMPR0~1;PGAMPK0~9;GAMP0								Default
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
B0H	0	0	vrp0[5:0]						02H
B1H	0	0	vrp1[5:0]						02H
B2H	0	0	vrp2[5:0]						02H
B3H	0	0	vrp3[5:0]						11H
B4H	0	0	vrp4[5:0]						16H
B5H	0	0	vrp5[5:0]						34H
B6H	0	prp0[6:0]						15H	
B7H	0	prp1[6:0]						32H	
B8H	0	0	0	pkp0[4:0]					11H
B9H	0	0	0	pkp1[4:0]					05H
BAH	0	0	0	pkp2[4:0]					18H
BBH	0	0	0	pkp3[4:0]					18H
BCH	0	0	0	pkp4[4:0]					18H
BDH	0	0	0	pkp5[4:0]					18H
BEH	0	0	0	pkp6[4:0]					1aH
BFH	0	0	0	pkp7[4:0]					0fH
C0H	0	0	0	pkp8[4:0]					18H
C1H	0	0	0	pkp9[4:0]					09H
C2H	0	0	0	gamp0[4:0]					00H
Description	Set the gray scale voltage to adjust the gamma characteristics of the TFT panel.								

5.3.10. NGAMVR0~5;NGAMPR0~1;NGAMPK0~9;GAMN0:D0H~E2H

Address	NGAMVR0~5;NGAMPR0~1;NGAMPK0~9;GAMN0								Default	
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0		
D0H	0	0	vrn0[5:0]							02H
D1H	0	0	vrn1[5:0]							02H
D2H	0	0	vrn2[5:0]							02H
D3H	0	0	vrn3[5:0]							11H
D4H	0	0	vrn4[5:0]							16H
D5H	0	0	vrn5[5:0]							34H
D6H	0	prn0[6:0]							15H	
D7H	0	prn1[6:0]							32H	
D8H	0	0	0	pkn0[4:0]						11H
D9H	0	0	0	pkn1[4:0]						05H
DAH	0	0	0	pkn2[4:0]						18H
DBH	0	0	0	pkn3[4:0]						18H
DCH	0	0	0	pkn4[4:0]						18H
DDH	0	0	0	pkn5[4:0]						18H
DEH	0	0	0	pkn6[4:0]						1aH
DFH	0	0	0	pkn7[4:0]						0fH
E0H	0	0	0	pkn8[4:0]						18H
E1H	0	0	0	pkn9[4:0]						09H
E2H	0	0	0	gamn0[4:0]						00H
Description	Set the gray scale voltage to adjust the gamma characteristics of the TFT panel.									

5.3.11. ENEXTC:FFH

FFh	ENEXTC																
	D7	D6	D5	D4	D3	D2	D1	D0	Default								
Command	1	1	1	1	1	1	1	1	FFH								
Parameter	0	0	0	0	0	0	page[1:0]		00H								
Description	<p>Config page. Write three times. The first time write 30h, the second time write 52h, the last time write page[1:0]. Write three times. The first time write 30h, the second time write 52h, the last time write the</p> <table border="1" data-bbox="692 698 1161 869"> <thead> <tr> <th>page</th> <th>Descriptions</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>select page0</td> </tr> <tr> <td>01</td> <td>select page1</td> </tr> <tr> <td>10</td> <td>select page2</td> </tr> </tbody> </table>									page	Descriptions	00	select page0	01	select page1	10	select page2
page	Descriptions																
00	select page0																
01	select page1																
10	select page2																

## 6. FUNCTIONS

### 6.1. Interface Type Selection

NV3051F1 support MIPI 1/2/3/4 Lane, which can be set by the IM[2:0] pins and LANSSEL.

Table 6-1, depicts the interface corresponding to IM[2:0] and LANSSEL pins.

External Pad Set			Configuration of MIPI Lane				
IM[2]	IM[1]	IM[0]	D0P/N	D1P/N	CLKP/N	D2P/N	D3P/N
0	0	0	D3P/N	D2P/N	CLKP/N	D1P/N	D0P/N
0	0	1	D3N/P	D2N/P	CLKN/P	D1N/P	D0N/P
0	1	0	D0P/N	D1P/N	CLKP/N	D2P/N	D3P/N
0	1	1	D0N/P	D1N/P	CLKN/P	D2N/P	D3N/P
1	0	0	D3P/N	D0P/N	CLKP/N	D1P/N	D2P/N
1	0	1	D3N/P	D0N/P	CLKN/P	D1N/P	D2N/P
1	1	0	D2P/N	D1P/N	CLKP/N	D0P/N	D3P/N
1	1	1	D2N/P	D1N/P	CLKN/P	D0N/P	D3N/P

Table 6-1

## 6.2. MIPI-DSI Interface

### 6.2.1. General description

The communication can be separated 2 different levels between the MCU and the display module:

- Interface Level : Low level communication
- Packet level : High level communication

### 6.2.2. Interface level communication

#### 6.2.2.1. General

The display module uses data and clock lane differential pairs for DSI. Both clock lane and data lane0 can be driven Low Power (LP) or High Speed (HS) mode. Data lane1/2/3 can be driven High Speed mode only.

-	Lane support mode	MPU(Host) NV3051F1(Slave)
Clock Lane	Unidirectional lane • High-Speed Clock only • Simplified Escape Mode (ULPS Only)	
Data Lane0	Bi-directional lane • Forward high-speed only • Bi-directional Escape Mode • Bi-direction LPDT	
Data Lane1/2/3	Unidirectional lane • Forward high-speed only • Simplified Escape Mode (ULPS Only)	

Table: Lane types and support mode

Low Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disable (A termination resistor of the receiver is disable) and it can be driven into a low power mode.

High Speed mode means that differential pairs (The termination resistor of the receiver is enable) are not used in the single end mode.

There are used different modes and protocols in each mode when there are wanted to transfer information from the MCU to the display module and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Lane Pair State Code	Line DC Voltage Levels		High Speed (HS)	Low-Power (LP)	
	Dn+ Line	Dn- Line	Burst Mode	Control Mode	Escape Mode
HS-0	Low (HS)	High (HS)	Differential-0	Note 1	Note 1
HS-1	High (HS)	Low (HS)	Differential-1	Note 1	Note 1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS-Request	Mark-0
LP-10	High (LP)	Low (LP)	Not Defined	LP-Request	Mark-1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2

Table: High Speed and Low-Power Lane Pair State Descriptions

**6.2.2.2. DSI-CLK lanes**

DSI-CLK+/- lanes can be driven into three different power modes: Low Power Mode (LPM LP-11), Ultra Low Power Mode (ULPM) or High Speed Clock Mode (HSCM).

Clock lanes are in a single end mode (LP = Low Power) when there is entering or leaving Low Power Mode(LPM) or Ultra Low Power Mode (ULPM).

Clock lanes are in the single end mode (LP = Low Power) when there is entering in or leaving out High Speed Clock Mode (HSCM).

These entering and leaving protocols are using clock lanes in the single end mode to generate an entering or leaving sequences.

The principal flow chart of the different clock lanes power modes is illustrated below.

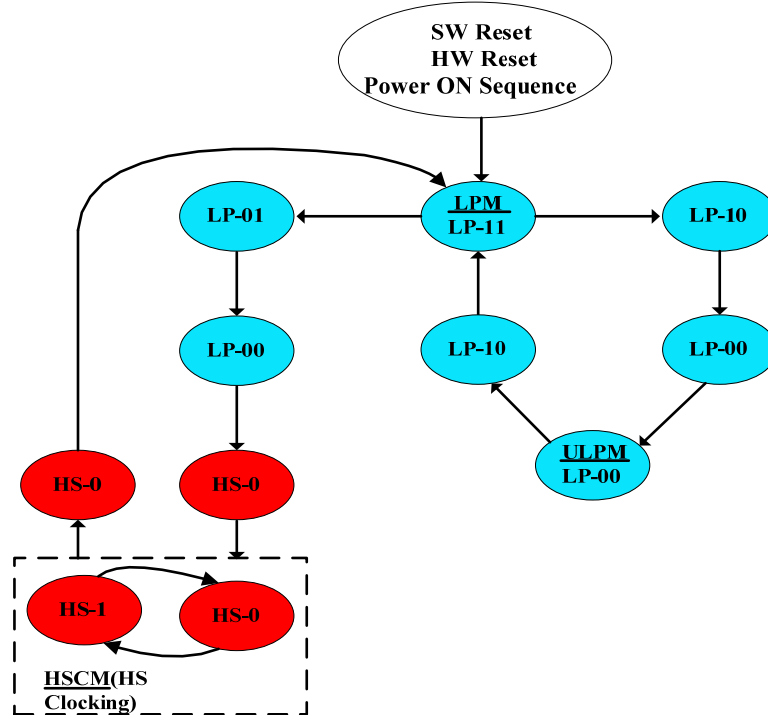


Figure: Clock Lanes Power Modes

Notes:

1. Low-Power Receivers (LP-Rx) of the lane pair are checking the LP-00 state code, when the Lane Pair is in the High Speed (HS) mode.
2. If Low-Power Receivers (LP-Rx) of the lane pair recognizes LP-11 state code, the lane pair returns to LP-11 of the Control Mode.

**Low Power Mode (LPM)**

DSI-CLK+/- lanes can be driven to the Low Power Mode (LPM), when DSI-CLK lanes are entering LP-11 State Code, in three different ways:

- 1) After SW Reset, HW Reset or Power On Sequence =>LP-11
- 2) After DSI-CLK+/- lanes are leaving Ultra Low Power Mode (ULPM, LP-00 State Code) =>LP-10 =>LP-11 (LPM). This sequence is illustrated below.

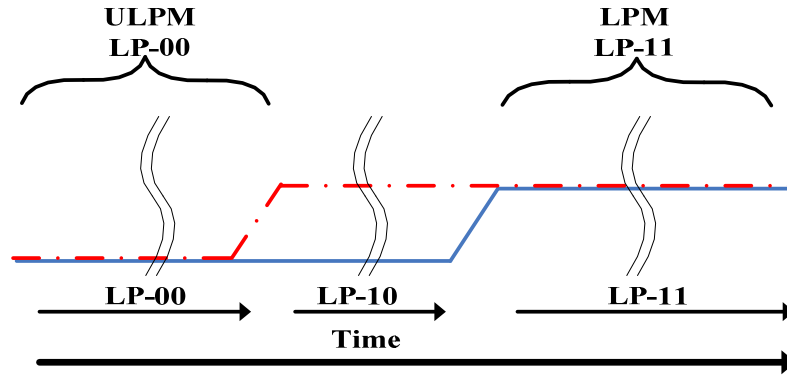


Figure: From ULPM to LPM

3) After DSI-CLK+/- lanes are leaving High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) =>HS-0 =>LP-11 (LPM). This sequence is illustrated below.

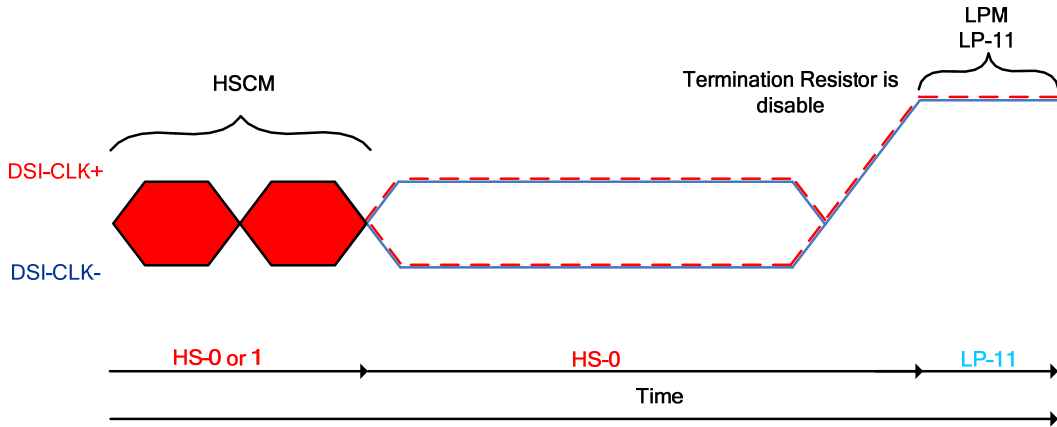


Figure: From HSCM to LPM



All three mode changes are illustrated a flow chart below.

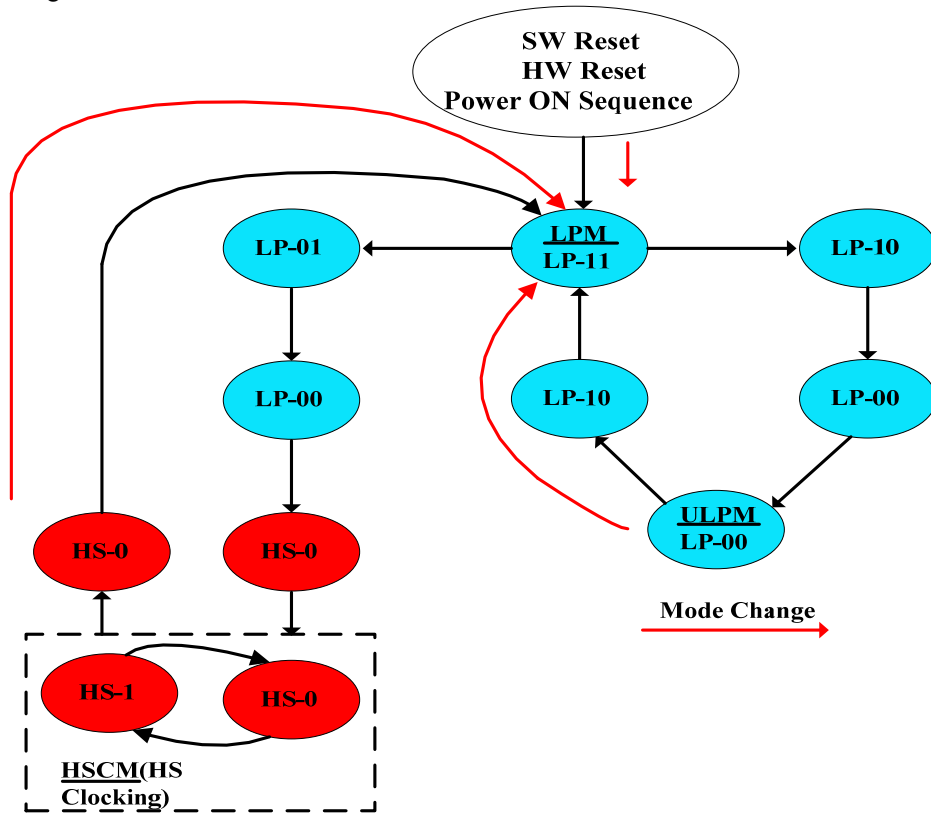


Figure: All three mode changes to LPM

### Ultra Low Power Mode (ULPM)

DSI-CLK+/- lanes can be driven to the High Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM). This sequence is illustrated below.

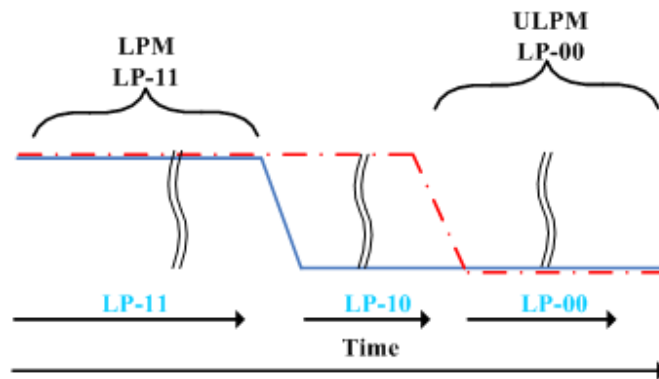


Figure: From LPM to ULPM

The mode change is also illustrated below:

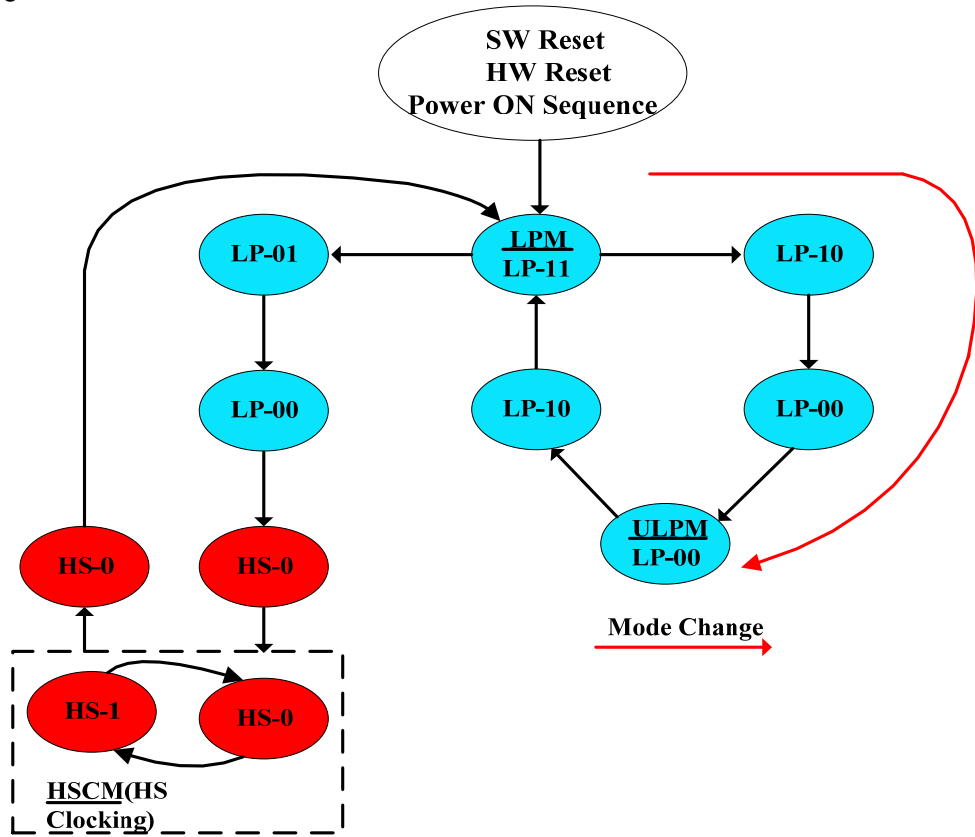


Figure: The mode change from LPM to ULPM

### High-speed Clock Mode (HSCM)

DSI-CLK+/- lanes can be driven to the High Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM). This sequence is illustrated below.

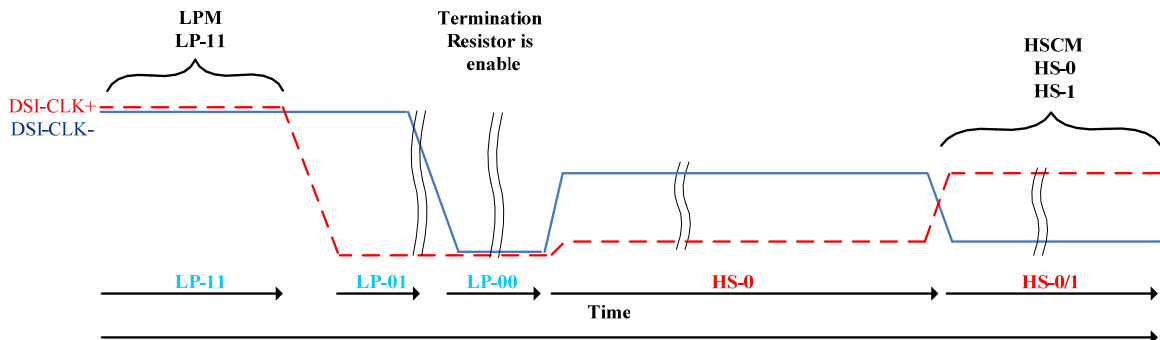


Figure: From LPM to HSCM

The mode change is also illustrated below:

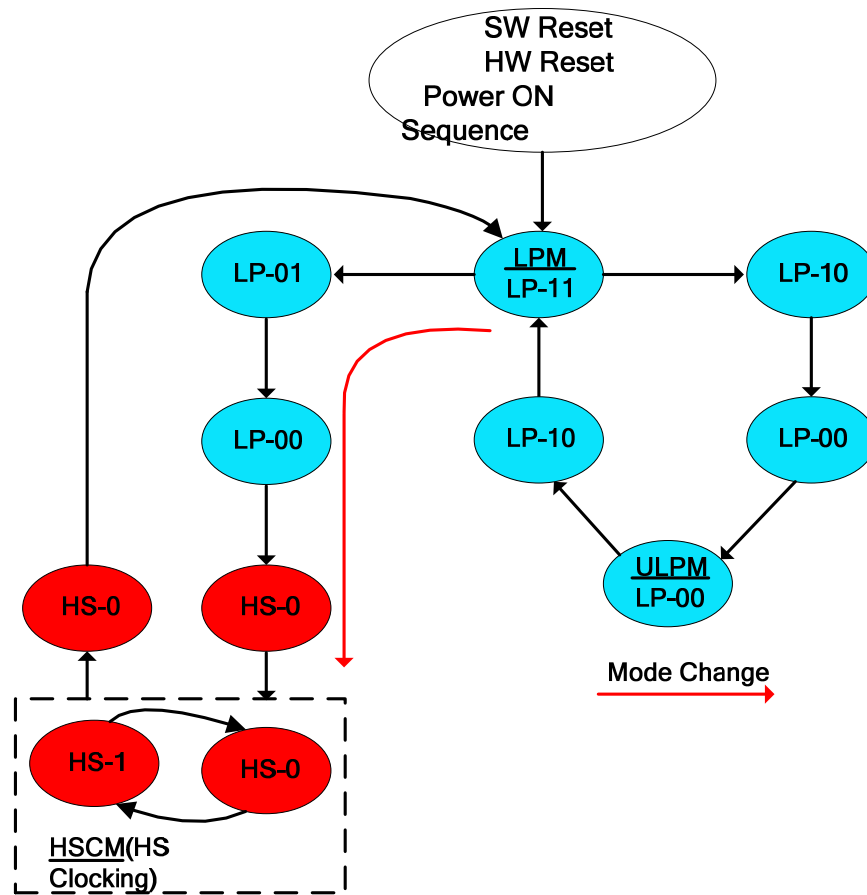


Figure: Mode change from LPM to HSCM

The high speed clock (DSI-CLK+/-) is started before high speed data is sent via DSI-Dn+/- lanes.  
 The high speed clock continues clocking after the high speed data sending has been stopped  
 The burst of the high speed clock consists of:

- Even number of transitions
- Start state is HS-0
- End state is HS-0

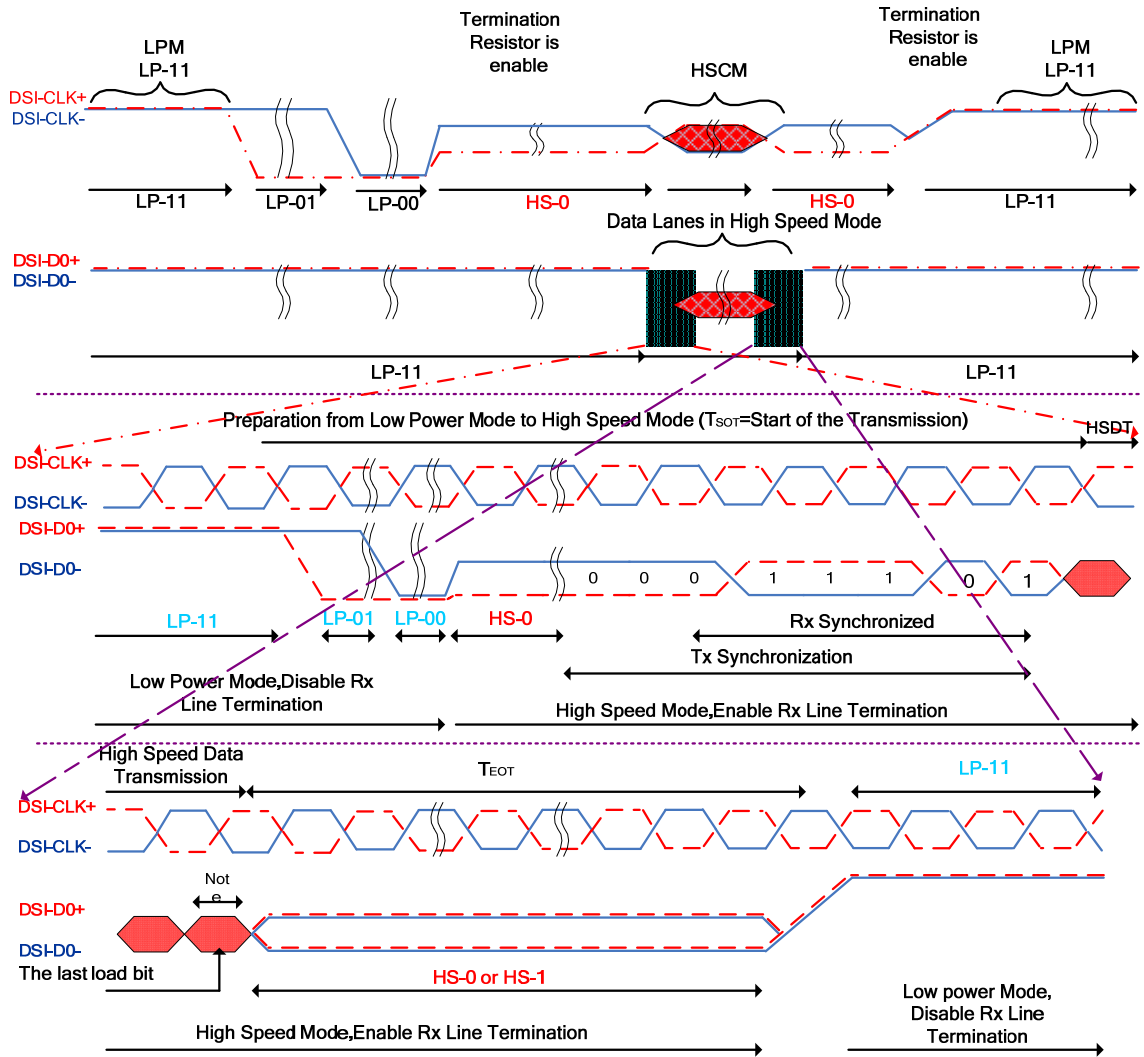


Figure: High speed clock burst

Note:

If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.

If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

### 6.2.3. DSI data lanes

#### 6.2.3.1. General

DSI-Dn+/- Data Lanes can be driven in different modes which are:

- Escape Mode (only support DSI\_D0 data lane pair)
- High-Speed Data Transmission (support all data lane pairs)
- Bus Turnaround Request (only support DSI\_D0 data lane pair)

These modes and their entering codes are defined on the following table.

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00	LP-00 =>LP-10 =>LP-11 (Mark-1)
High-Speed Data Transmission	LP-11 =>LP-01 =>LP-00 =>HS-0	(HS-0 or HS-1) =>LP-11
Bus Turnaround Request	LP-11 =>LP-10 =>LP-00 =>LP-10 =>LP-00	High-Z, Note

Table: Entering and leaving sequences

#### 6.2.3.2. Escape modes

Escape mode is a special mode of operation for Data Lanes using Low-Power states. With this mode some additional functionality becomes available. Escape mode operation shall be supported in the Forward direction and Reverse direction.

The basic sequence of the Escape Mode is as follow

- Start: LP-11
- Escape Mode Entry: LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Escape Command, which is coded, when one of the data lanes is changing from low-to-high-to-low then this changed data lane is presenting a value of the current data bit.
- A payload stream if it is needed
- Exit Escape (Mark-1) LP-00 =>LP-10 =>LP-11
- End: LP-11

For Data Lane0, once Escape mode is entered, the transmitter shall send an 8-bit entry command to indicate the requested action.

All currently available Escape mode commands and actions are list below.

- Send or receive “Low-Power Data Transmission” (LPDT)
- Drive data lanes to “Ultra-Low Power State” (ULPS)
- Indicate “Remote Application Reset” (RAR), which is resetting the display module (same as S/W Reset function)
- Indicate “Tearing Effect” (TEE), which is used for a TE line event from the display module to the MCU,
- Indicate “Acknowledge” (ACK), which is used for a non-error event from the display module to the MCU.

The Stop state shall be used to exit Escape mode and cannot occur during Escape mode operation because of the Spaced-One-Hot encoding.

Stop state immediately returns the Lane to Control mode. If the entry command doesn't match a supported command, that particular Escape mode action shall be ignored and the receive side waits until the transmit side returns to the Stop state.

For Data Lane1 and 2, only support ULPS Escape mode commands.

- Drive data lanes to “Ultra-Low Power State” (ULPS)

The basic construction is illustrated below:

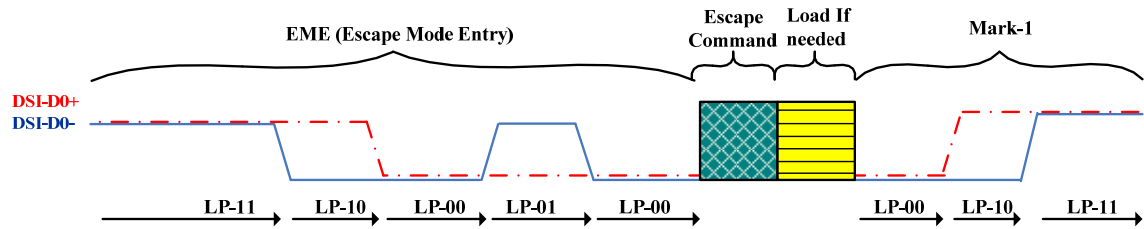


Figure: General Escape mode sequence

The number of the different Escape Commands is eight. These eight different Escape Commands can be divided 2 different groups: Mode or Trigger. Escape command groups are defined below.

Escape Command	Command Type Mode/Trigger	Entry Command Pattern (First Bit => Last Bit Transmitted)
Low-Power Data Transmission	Mode	1110 0001 bin
Ultra-Low Power Mode	Mode	0001 1110 bin
Remote Application Reset	Trigger	0110 0010 bin
Tearing Effect	Trigger	0101 1101 bin
Acknowledge	Trigger	0010 0001 bin

Table: Escape commands

The MCU is informing to the display module that it is controlling data lanes (DSI-D0+/-) with the mode e.g.

The MCU can inform to the display module that it can put data lanes in the low power mode.

The MCU is waiting from the display module event information, which has been set by the MCU, with the trigger e.g. when the display module reaches a new V-synch, the display module sent to the MCU a TE trigger (TEE), if the MCU has been requested it.

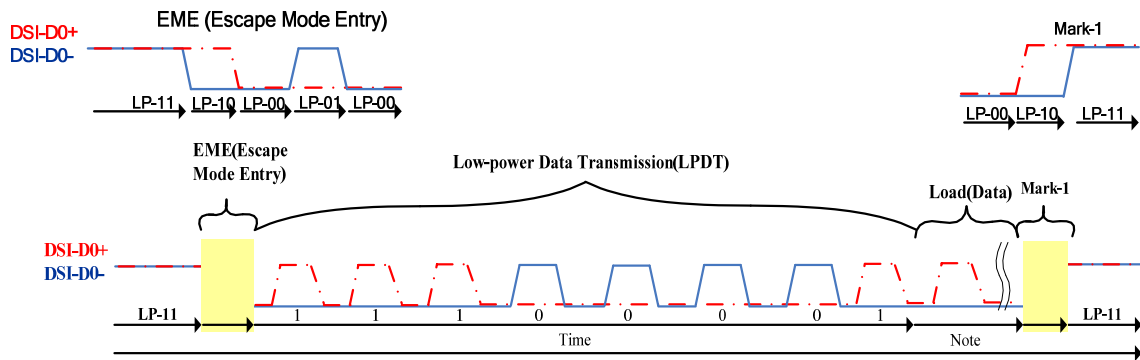
**Low-Power Data Transmission (LPDT)**

The MCU can send data to the display module in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command has been sent to the display module. The display module is also using the same sequence when it is sending data to the MCU.

The Low Power Data Transmission (LPDT) is using a following sequence:

- Start: LP-11
- Escape Mode Entry: LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Low-Power Data Transmission (LPDT) command in Escape Mode: 1110 0001 (First to Last bit)
- Payload (Data):
  - One or more bytes
  - Data lanes are in pause mode when data lanes are stopped (Both lanes are low) between bytes
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



Note: Load(Data) is presenting that the first bit is logical "1" in this example.

Figure: Low-power data transmission

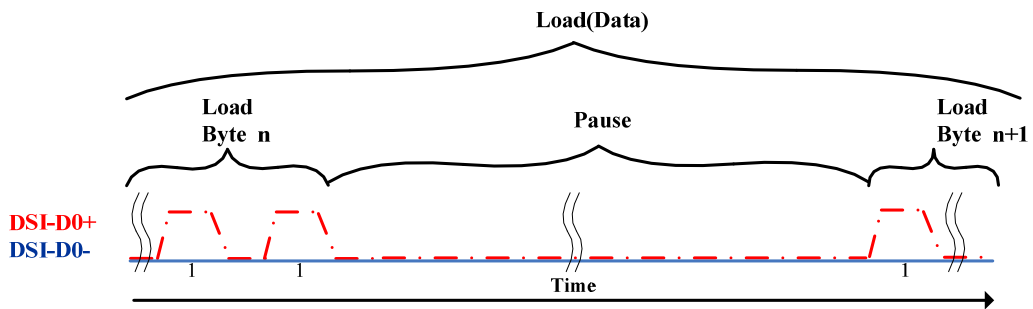


Figure: Pause (example)

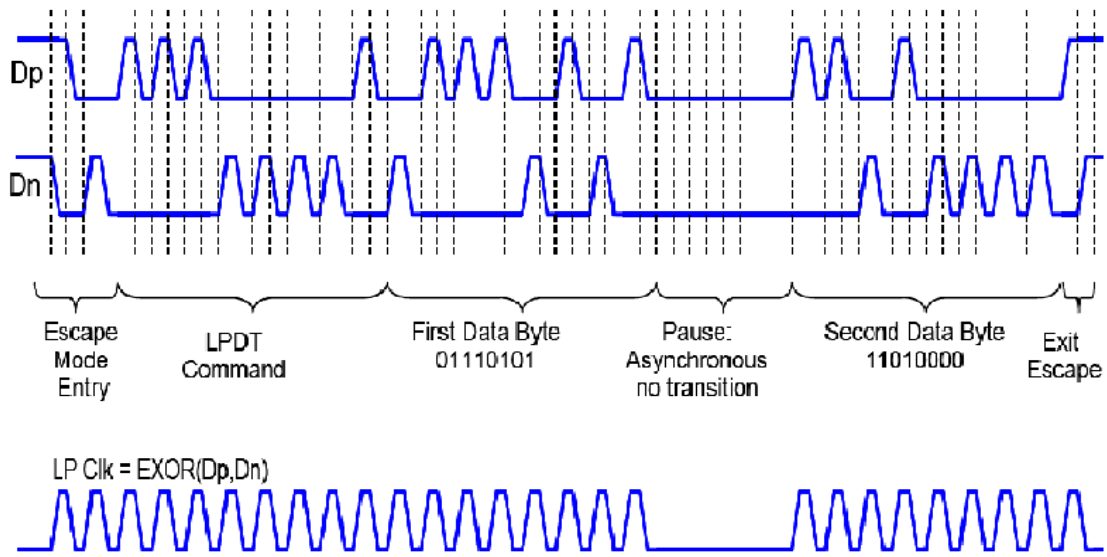


Figure: Two Data Byte Low-Power Data Transmission Example

### Ultra-Low Power State (ULPS)

The MCU can force data lanes in Ultra-Low Power State (ULPS) mode when data lanes are entering in Escape Mode.

The Ultra-Low Power State (ULPS) is using a following sequence:

- Start: LP-11
- Escape Mode Entry : LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit)
- Ultra-Low Power State (ULPS) when the MCU is keeping data lanes low
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

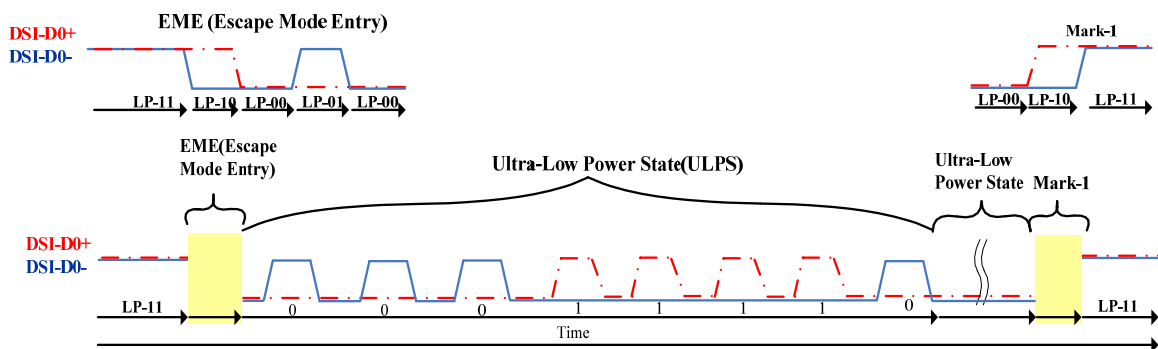


Figure: Ultra-low power state(ULPS)



### Remote Application Reset (RAR)

The MCU can inform to the display module that it should be reseted in Remote Application Reset (RAR) trigger when data lanes are entering in Escape Mode. The Remote Application Reset is using a following sequence:

- Start: LP-11
- Escape Mode Entry : LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

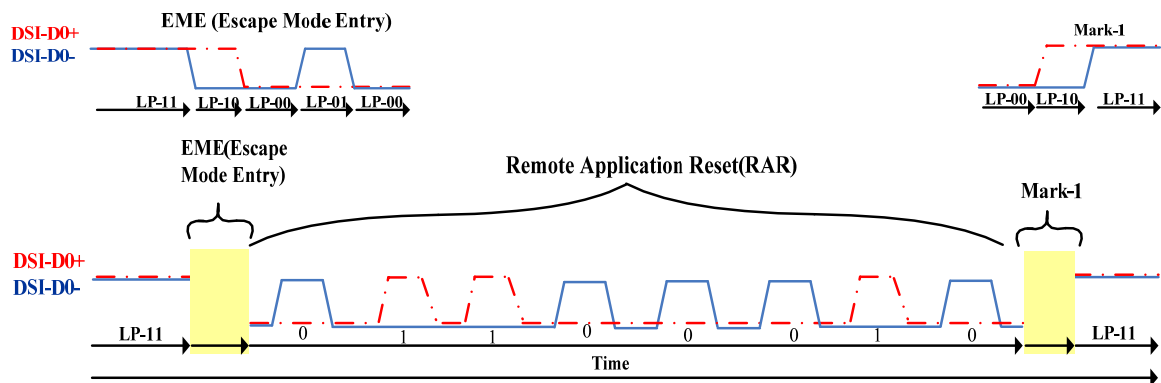


Figure: Remote Application Reset (RAR)

### Tearing Effect (TEE)

The display module can inform to the MCU when a tearing effect event (New V-synch) has been happen on the display module by Tearing Effect (TEE).

The Tearing Effect (TEE) is using a following sequence:

- Start: LP-11
- Escape Mode Entry: LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Tearing Effect (TEE) trigger in Escape Mode: 0101 1101 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11



### 6.2.3.3. High-Speed Data Transmission (HSDT)

#### Entering High-Speed Data Transmission (T<sub>sot</sub> of HSDT)

The display module is entering High-Speed Data Transmission (HSDT) when Clock lanes DSI-CLK+/- have already been entered in the High-Speed Clock Mode (HSCM) by the MCU. See more information on chapter “High-Speed Clock Mode (HSCM)”.

Data lanes DSI-D0+/- of the display module are entering (T<sub>sot</sub>) in the High-Speed Data Transmission(HSDT) as follows

- Start: LP-11
- HS-Request: LP-01
- HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)
- Rx Synchronization: 011101 (Tx (= MCU) Synchronization: 0001 1101)
- End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This same entering High-Speed Data Transmission (T<sub>sot</sub> of HSDT) sequence is illustrated below.

#### Preparation from Low Power Mode to High Speed Mode( T<sub>sot</sub>=Start of the Transmission)

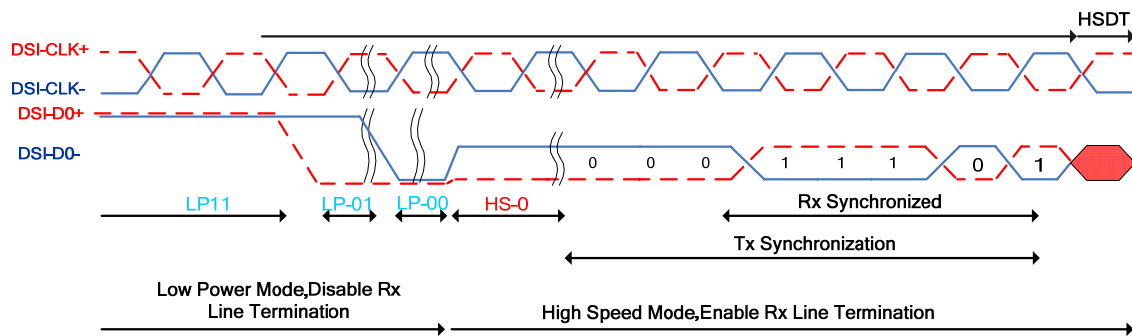


Figure: T<sub>sot</sub> of HSDT

#### Leaving High-Speed Data Transmission (T<sub>EOt</sub> of HSDT)

The display module is leaving the High-Speed Data Transmission (T<sub>EOt</sub> of HSDT) when Clock lanes DSI-CLK+/- are in the High-Speed Clock Mode (HSCM) by the MCU and this HSCM is kept until data lanes DSI-D0+/- are in LP-11 mode. See more information on chapter “High-Speed Clock Mode (HSCM)”.

Data lanes DSI-D0+/- of the display module are leaving from the High-Speed Data Transmission (T<sub>EOt</sub> of HSDT) as follows

- Start: High-Speed Data Transmission (HSDT)
- Stops High-Speed Data Transmission
- MCU changes to HS-1, if the last load bit is HS-0
- MCU changes to HS-0, if the last load bit is HS-1
- End: LP-11 (Rx: Lane Termination Disable)

This same leaving High-Speed Data Transmission (TEOT of HSDT) sequence is illustrated below

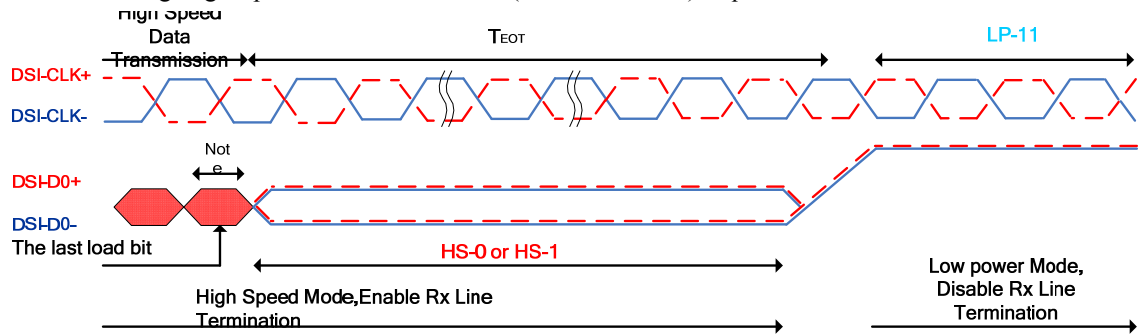


Figure: TEOT of HSDT

Note:

If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.

If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

### Burst of the High-Speed Data Transmission (HSDT)

The burst of the high-speed data transmission (HSDT) can consist of one data packet or several data packets. These data packets can be Long (Lpa) or Short (Spa) packets. These packets are defined on chapter “Short Packet (Spa) and Long Packet (Lpa) Structures”.

These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated for reference purposes below.

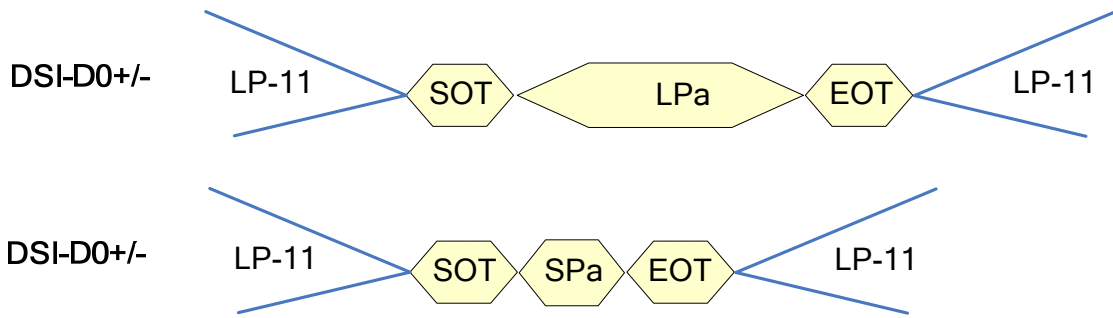


Figure: Single packet in HSDT

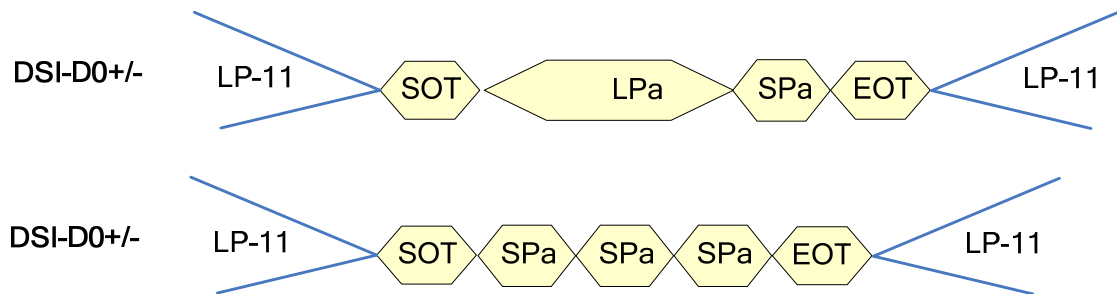


Figure: Multiple packets in HSDT



Figure: Packets with EoT package in HSDT

Abbreviation	Explanation
LP-11	Low Power Mode, Data lanes are '1's (Stop Mode)
SOT	Start of the Transmission
Lpa	Long Packet
Spa	Short Packet
EOT	End of the Transmission

Table: Abbreviations

#### 6.2.3.4. Bus Turnaround (BTA)

The MCU or display module, which is controlling DSI-D0+/- Data Lanes, can start a bus turnaround procedure when it wants information from a receiver, which can be the MCU or display module.

The MCU and display module are using the same sequence when this bus turnaround procedure is used.

This sequence is described for reference purposes, when the MCU wants to do the bus turnaround procedure to the display module, as follows.

- Start (MCU): LP-11
- Turnaround Request (MCU): LP-11 =>LP-10 =>LP-00 =>LP-10 =>LP-00
- The MCU waits until the display module is starting to control DSI-D0+/- data lanes and the MCU stops to control DSI-D0+/- data lanes (= High-Z)
- The display module changes to the stop mode: LP-00 =>LP-10 =>LP-11

The same bus turnaround procedure (From the MCU to the display module) is illustrated below.

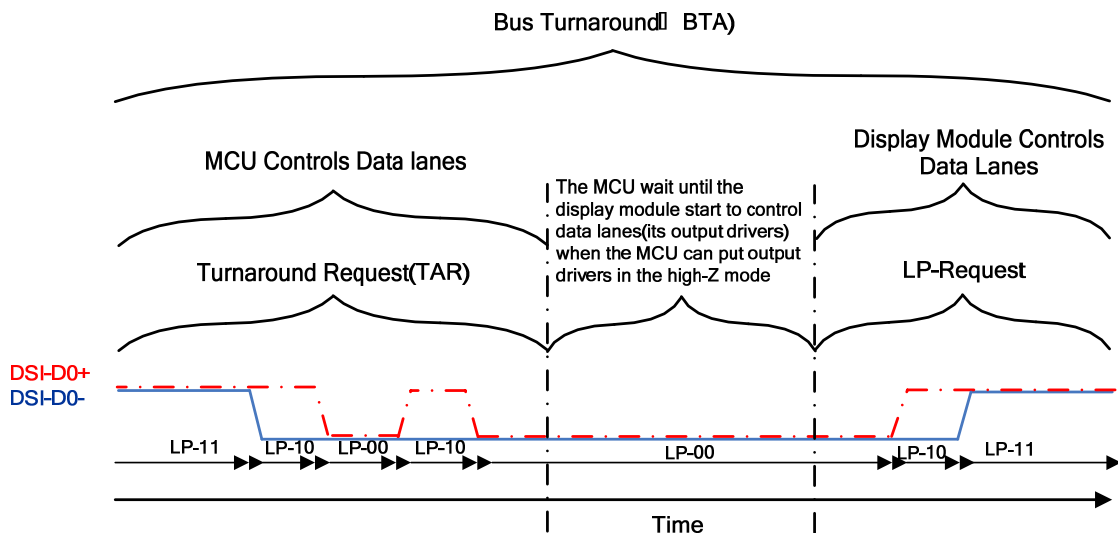


Figure: Bus turnaround procedure

**6.2.3.5. Two Data-lane High Speed Transmission**

Since a HS transmission is composed of an arbitrary number of bytes that may not be an integer multiple of the number of lanes, one lane may run out of data before the other. Therefore, the lane management layer, as it buffers up the final set of less-than-2 bytes, de-asserts its “valid data” signal into all lanes for which there’s no further data.

Although all lanes start simultaneously with parallel SoTs, each lane operates independently and may complete the HS transmission before the other lane, sending an EoT one cycle (byte) earlier.

The two PHYs on the receiving end of the link collect bytes in parallel and feed them into the lane management layer. The lane management layer reconstructs the original sequence of bytes in the transmission.

Below Figure shows the way a HS transmission can terminate for two data-lane HS transmission.

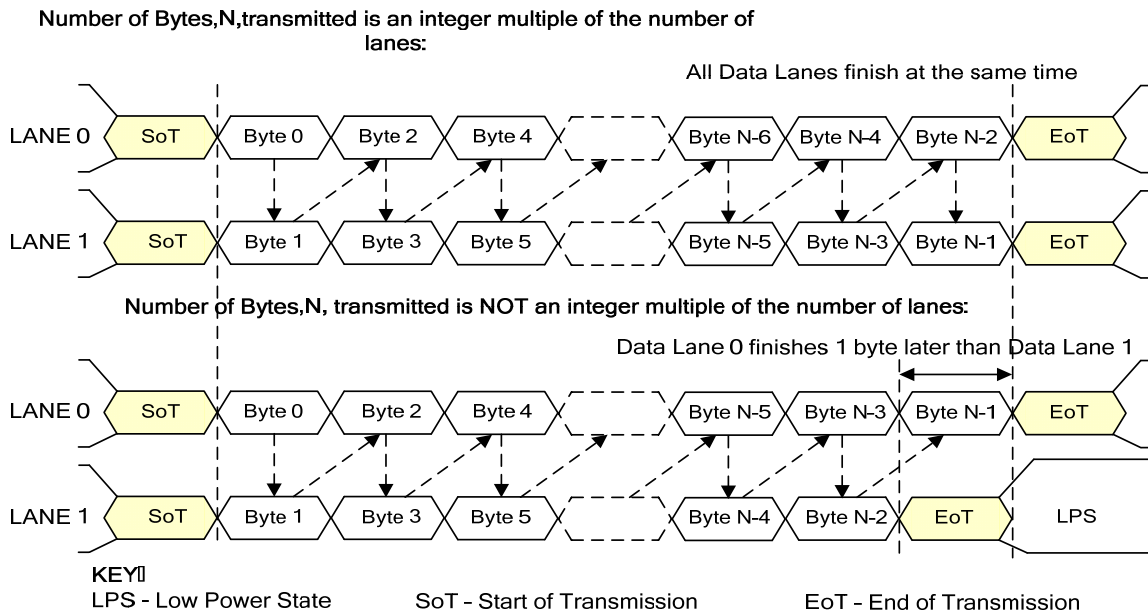


Figure: Two data-lane HS transmission example

**6.2.3.6. Three data-lane high speed transmission**

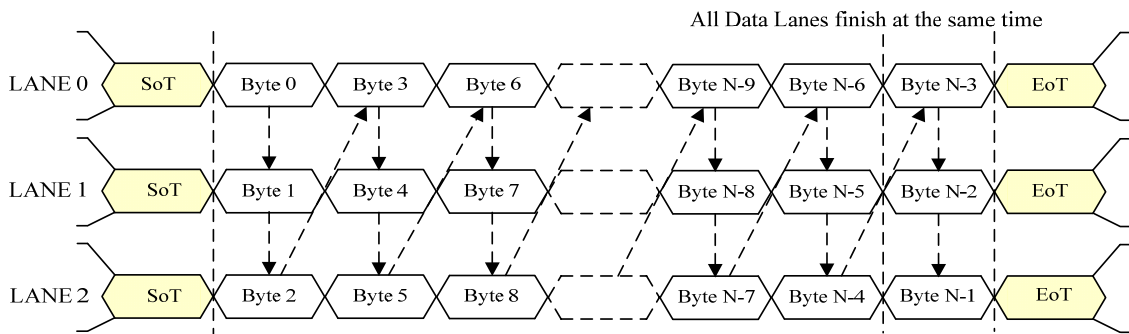
Since a HS transmission is composed of an arbitrary number of bytes that may not be an integer multiple of the number of Lanes, some Lanes may run out of data before others. Therefore, the Lane Management layer, as it buffers up the final set of less-than-N bytes, de-asserts its “valid data” signal into all Lanes for which there is no further data.

Although all Lanes start simultaneously with parallel SoTs, each Lane operates independently and may complete the HS transmission before the other Lanes, sending an EoT one cycle (byte) earlier.

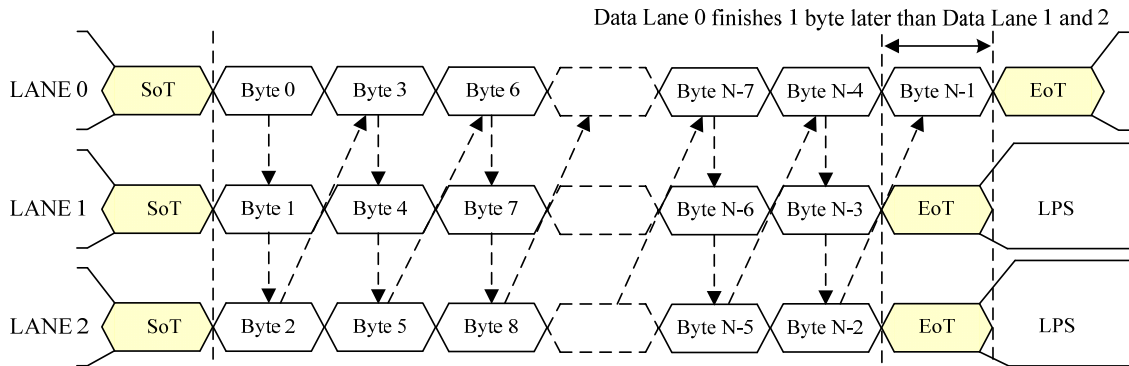
The N PHYs on the receiving end of the Link collect bytes in parallel and feed them into the Lane Management layer. The Lane Management layer reconstructs the original sequence of bytes in the transmission.

Below Figure illustrate a variety of ways a HS transmission can terminate for different number of Lanes and packet lengths.

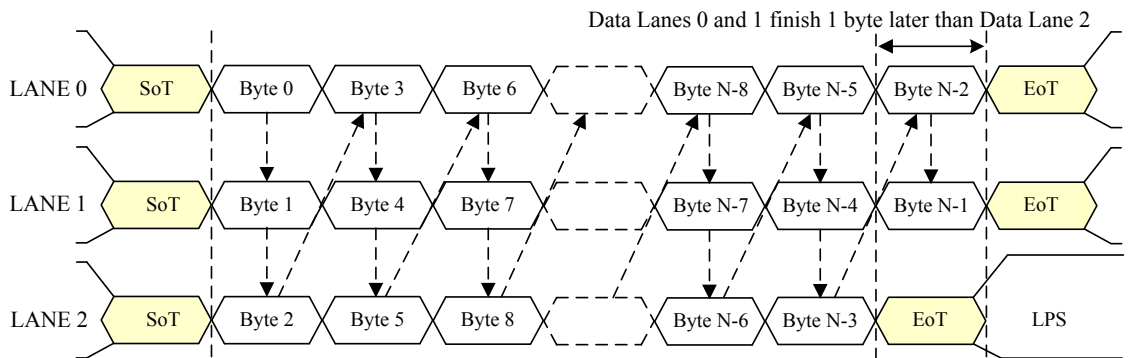
**Number of Bytes,N,transmitted is an integer multiple of the number of lanes:**



**Number of Bytes,N,transmitted is NOT an integer multiple of the number of lanes (Example 1):**



**Number of Bytes,N,transmitted is NOT an integer multiple of the number of lanes(Example 2):**



**6.2.4. Packet level communication**

**6.2.4.1. Short Packet (Spa) and Long Packet (Lpa) structures**

Short Packet (Spa) and Long Packet (Lpa) are always used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDDT) modes. The lengths of the packets are

- Short Packet (Spa): 4 bytes
- Long Packet (Lpa): From 6 to 65,541 bytes

The type (Spa or Lpa) of the packet can be recognized from their package headers (PH).

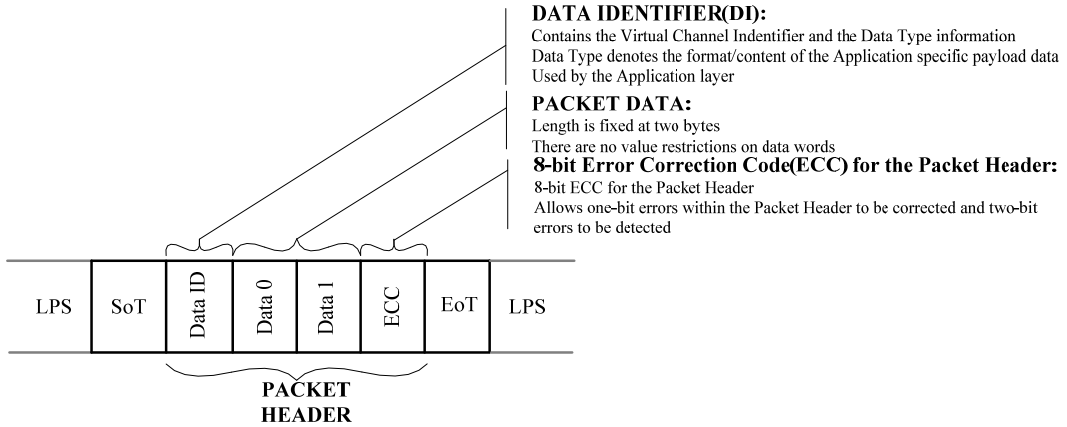


Figure: Short packet structure

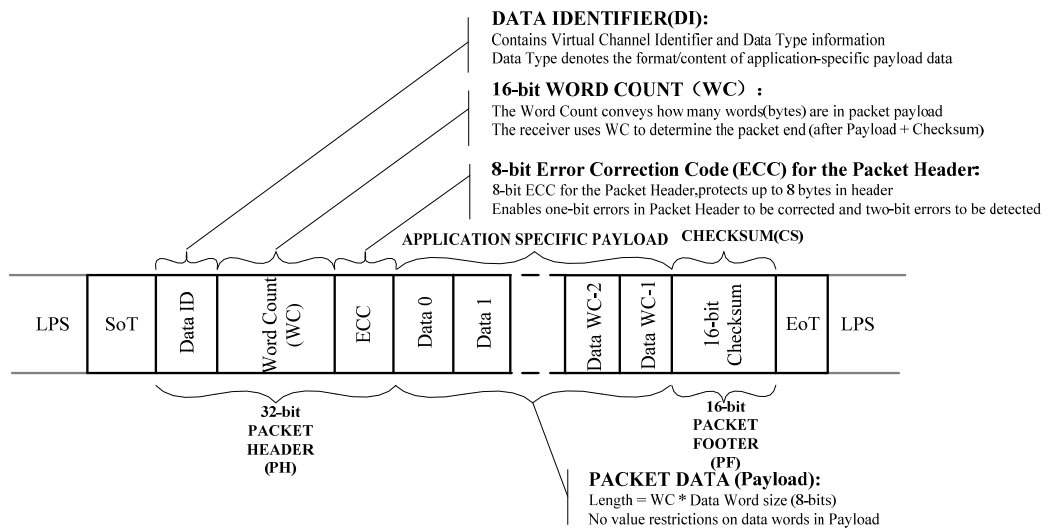


Figure: Long packet structure

Note: “Short Packet (Spa) Structure” and “Long Packet (Lpa) Structure” are presenting a single packet sending (= Includes LP-11, SoT and EoT for each packet sending).

The other possibility is that there is not needed SoT, EoT and LP-11 between packets if packets have sent in multiple packet format. e.g.:

- LP-11 =>SoT =>Spa =>Lpa =>Spa =>Spa =>EoT =>LP-11
- LP-11 =>SoT =>Spa =>Spa =>Spa =>EoT =>LP-11
- LP-11 =>SoT =>Lpa =>Lpa =>Lpa =>EoT =>LP-11



**Bit Order of the Byte on Packets**

All packet data traverses the interface as bytes. Sequentially, a transmitter shall send data LSB first, MSB last. For packets with multi-byte fields, the least significant byte shall be transmitted first unless otherwise specified.

Below Figure shows a complete Long packet data transmission. Note, the figure shows the byte values in standard positional notation, i.e. MSB on the left and LSB on the right, while the bits are shown in chronological order with the LSB on the left, the MSB on the right and time increasing left to right.

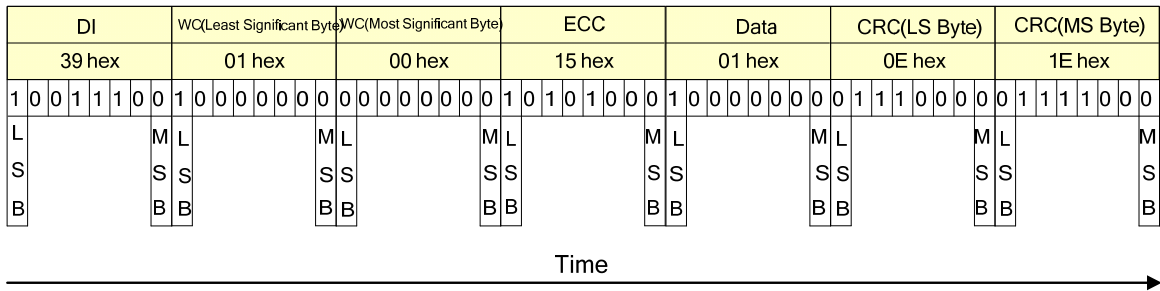


Figure: Bit order of the byte on packets

**Byte Order of the Multiple Byte Information on Packets**

Byte order of the multiple bytes information, what is used on packets, is that the Least Significant (LS) Byte of the information is sent in the first and the Most Significant (MS) Byte of the information is sent in the last. E.g. Word Count (WC) consists of 2 bytes (16 bits) when the LS byte is sent in the first and the MS byte is sent in the last. This same order is illustrated for reference purposes below.

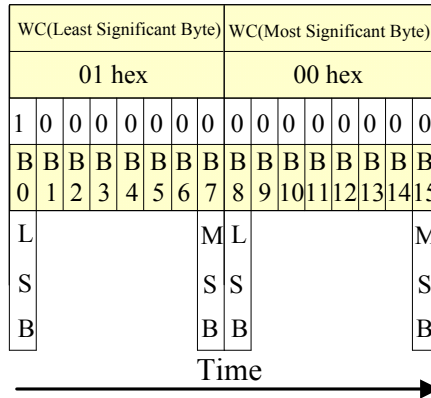


Figure: Byte order of the multiple byte information on packets

**Packet Head (PH)**

The packet header is always consisting of 4 bytes. The content of these 4 bytes are different if it is used to Short Packet (Spa) or Long Packet (Lpa).

Short Packet (Spa):

- 1<sup>st</sup> byte: Data Identification (DI) => Identification that this is Short Packet (Spa)
- 2<sup>nd</sup> and 3<sup>rd</sup> bytes: Packet Data (PD), Data 0 and 1
- 4<sup>th</sup> byte: Error Correction Code (ECC)

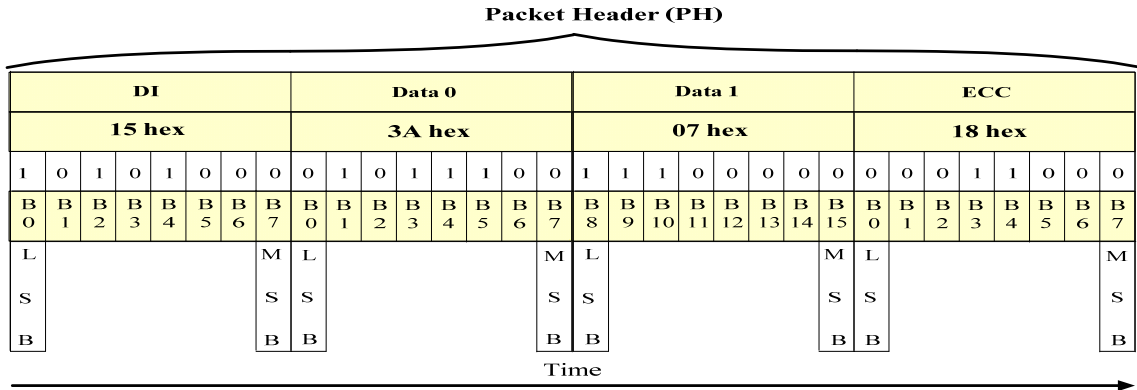


Figure: Packet head on short packet

Long Packet (Lpa):

- 1<sup>st</sup> byte: Data Identification (DI) => Identification that this is Long Packet (Lpa)
- 2<sup>nd</sup> and 3<sup>rd</sup> bytes: Word Count (WC)
- 4<sup>th</sup> byte: Error Correction Code (ECC)

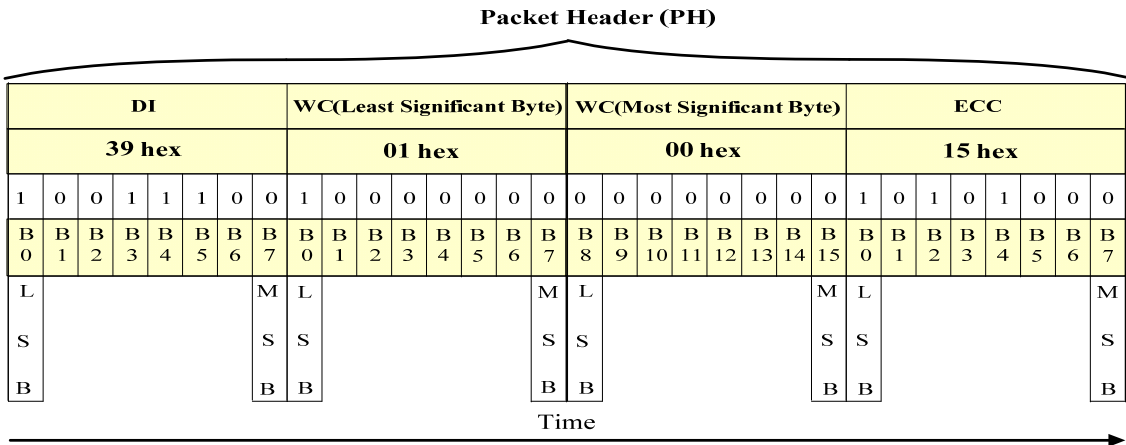


Figure: Packet head on long packet

**Data Identification**

Data Identification (DI) is a part of Packet Header (PH) and it consists of 2 parts:

- Virtual Channel (VC), 2 bits, DI[7..6]
- Data Type (DT), 6 bits, DI[5...0]

The Data Identification (DI) structure is illustrated on a table below.

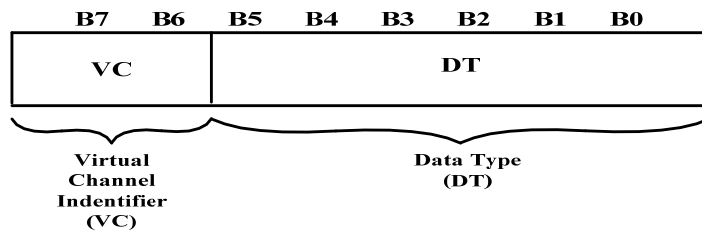


Table: Data identification structure

Data Identification (DI) is illustrated on Packet Header (PH) for reference purposes below.

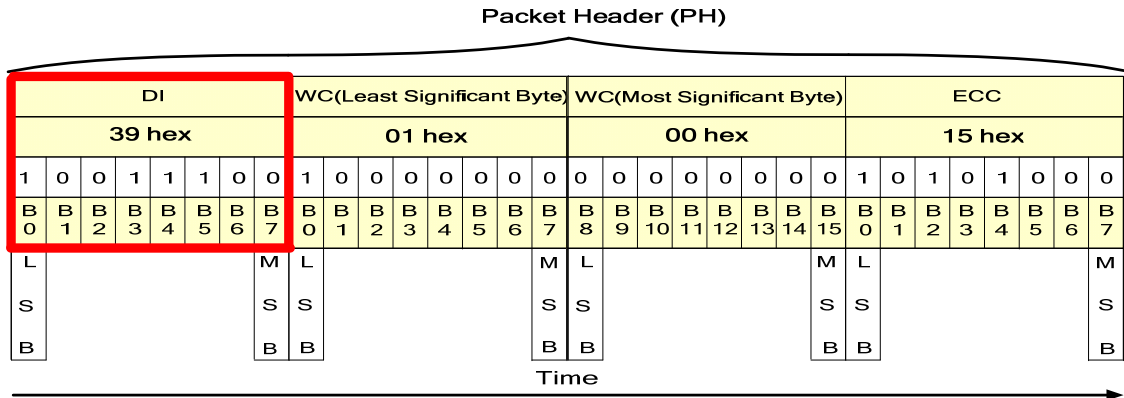


Figure: Data identification of the packet head

### Virtual Channel (VC)

A processor may service up to four peripherals with tagged commands or blocks of data, using the Virtual Channel ID field of the header for packets targeted at different peripherals.

Virtual Channel (VC) is a part of Data Identification (DI[7...6]) structure and it is used to address where a packet is wanted to send from the MCU. Bits of the Virtual Channel (VC) are illustrated for reference purposes below.

**NV3051F1 only support VC code=00, package with other VC code(01/10/11) will be filter out.**

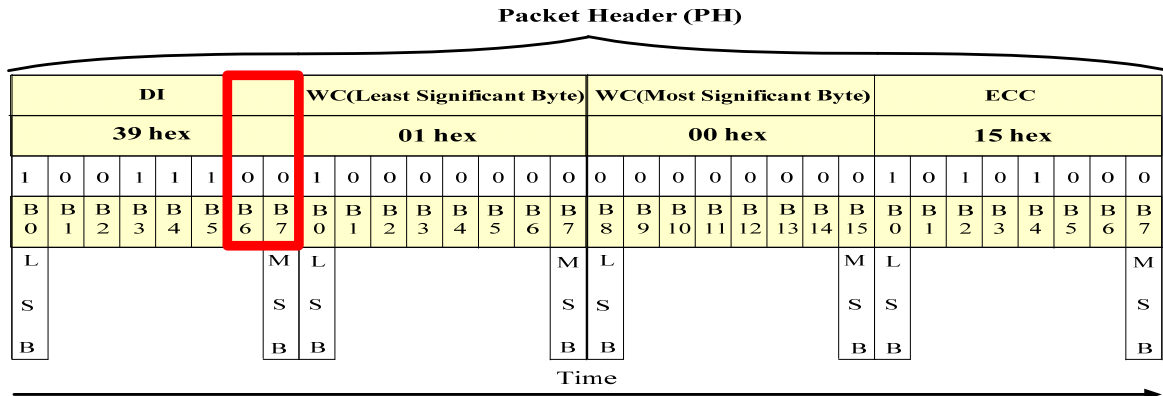


Figure: Virtual channel on the packet head

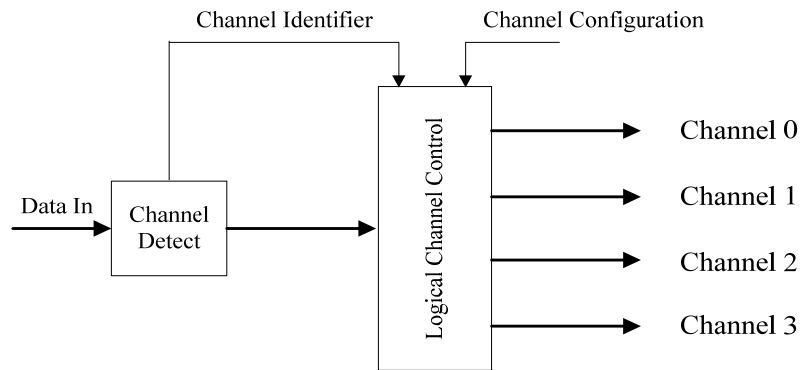


Figure: Virtual channel block diagram (receiver case)

**Data Type (DT)**

Data Type (DT) is a part of Data Identification (DI[5...0]) structure and it is used to define a type of the used data on a packet.

Bits of the Data Type (DT) are illustrated for reference purposes below.

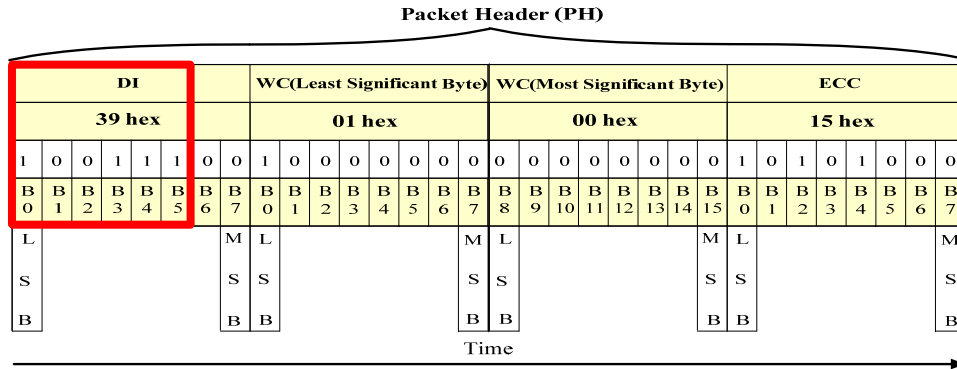


Figure: Data type on the packet head

This Data Type (DT) also defines what the used packet is: Short Packet (Spa) or Long Packet (Lpa). Data Types (DT) are different from the MCU to the display module (or other devices) and vice versa. These Data Type (DT) are defined on tables below.

<b>From the MCU to the Display module</b>		
Data Type(HEX)	Data Type(Binary)	Description
01h	00 0001	Sync Event, V Sync Start
11h	01 0001	Sync Event, V Sync End
21h	10 0001	Sync Event, H Sync Start
31h	11 0001	Sync Event, H Sync End
08h	00 1000	End of Transmission (EoT) packet
02h	00 0010	Color Mode (CM) Off Command
12h	01 0010	Color Mode (CM) On Command
22h	10 0010	Shut Down Peripheral Command
32h	11 0010	Turn On Peripheral Command
03h	00 0011	Generic Short WRITE, no parameters
13h	01 0011	Generic Short WRITE, 1 parameters
23h	10 0011	Generic Short WRITE, 2 parameters
04h	00 0100	Generic READ, no parameters
14h	01 0100	Generic READ, 1 parameters
24h	10 0100	Generic READ, 2 parameters
05h	00 0101	DCS WRITE, no parameters
15h	01 0101	DCS WRITE, 1 parameters
06h	00 0110	DCS READ, no parameters
37h	11 0111	Set Maximum Return Packet Size
09h	00 1001	Null Packet, no data

19h	01 1001	Blanking Packet, no data
29h	10 1001	Generic Long Write
39h	11 1001	DCS Long Write/Write_LUT Command packet
0Eh	00 1110	Packet Pixel Stream, 16-bit RGB, 5-6-5 Format
2Eh	10 1110	Loosely Packet Pixel Stream, 18-bit RGB, 6-6-6 Format
3Eh	11 1110	Packet Pixel Stream, 24-bit RGB, 8-8-8 Format

Table: Data type from the MCU to the display module

From the Display Module to the MCU		
Data Type(HEX)	Data Type(Binary)	Description
02h	00 0010	Acknowledge & Error Report
11h	01 0001	Generic Short READ Response, 1 byte returned
21h	10 0001	DCS Short READ Response, 1 byte returned

Table: Data type from the display module to the MCU

The receiver is ignored other Data Type (DT) if they are not defined on tables above. Host send “Generic Read” data type, NV3051F1 will return DCS Read package to Host.

**Packet data on the short packet**

Packet Data (PD) of the Short Packet (Spa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Short Packet (Spa) is wanted to send.

Packet Data (PD) of the Short Packet (Spa) consists of 2 data bytes: Data 0 and Data 1.

Packet Data (PD) sending order is that Data 0 is sent in the first and the Data 1 is sent in the last.

Bits of Data 1 are set to 00h, if the information length is 1 byte.

Packet Data (PD) of the Short Packet (Spa), when the length of the information is 1 or 2 bytes are illustrated for reference purposes below.

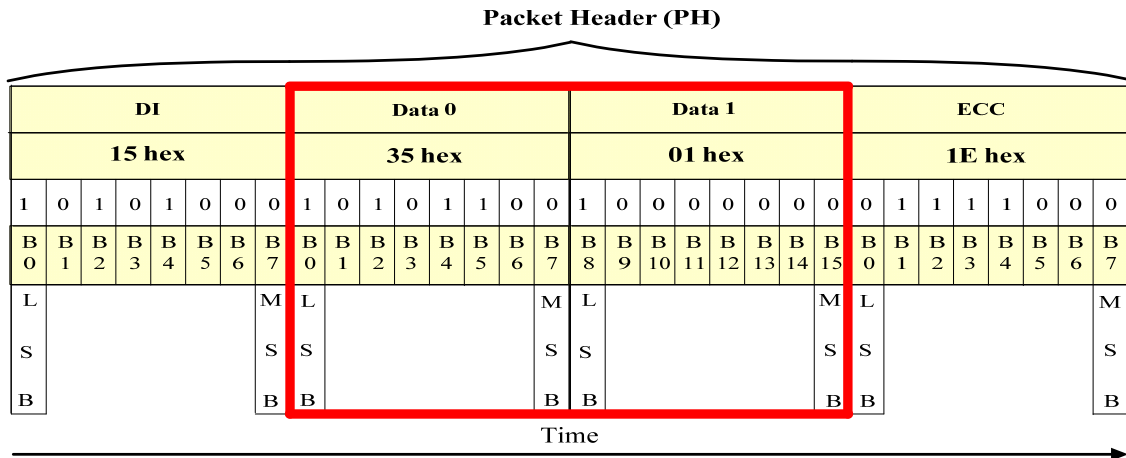


Figure: Packet data on the short packet, 2 bytes information

Packet Data (PD) information:

- Data 0: 10hex
- Data 1: 00hex (Null)

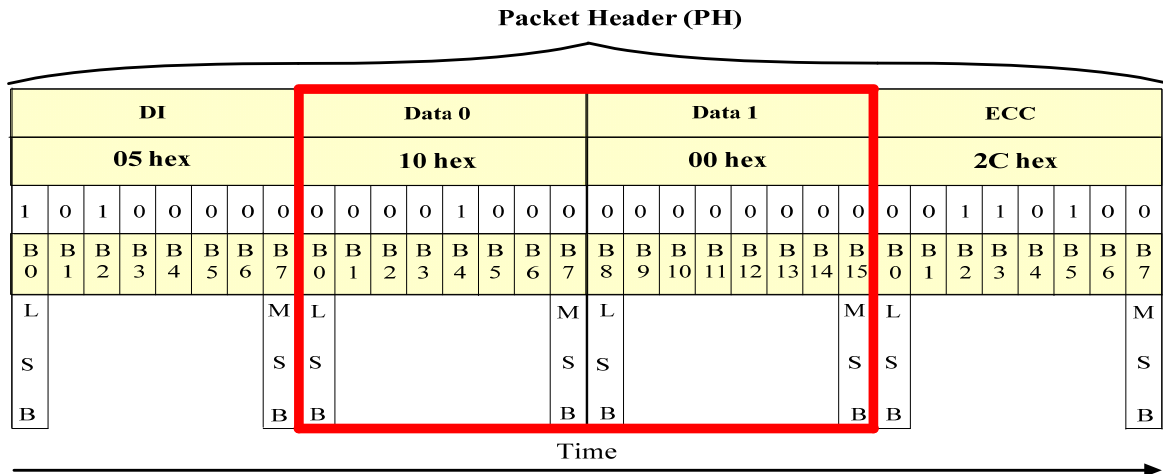


Figure: Packet data on the short packet, 1 bytes information

**Word count on the long packet**

Word Count (WC) of the Long Packet (Lpa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Long Packet (Lpa) is wanted to send.

Word Count (WC) indicates a number of the data bytes of the Packet Data (PD) what is wanted to send after Packet Header (PH) versus Packet Data (PD) of the Short Packet (Spa) is placed in the Packet Header (PH).

Word Count (WC) of the Long Packet (Lpa) consists of 2 bytes.

These 2 bytes of the Word Count (WC) sending order is that the Least Significant (LS) Byte is sent in the first and the Most Significant (MS) Byte is sent in the last.

Word Count (WC) of the Long Packet (Lpa) is illustrated for reference purposes below.

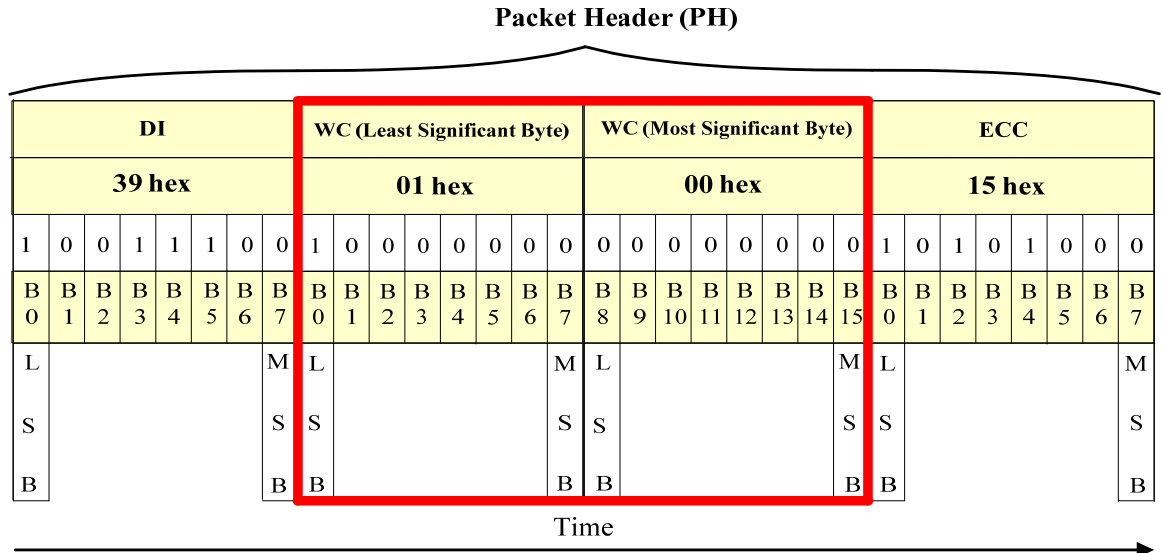


Figure: Word count on the long packet

**Error Correction Code (ECC)**

Error Correction Code (ECC) is a part of Packet Header (PH) and its purpose is to identify an error or errors:

- Short Packet (Spa): Data Identification (DI) and Packet Data (PD) bytes (24 bits: D[23...0])
- Long Packet (Lpa): Data Identification (DI) and Word Count (WC) bytes (24 bits: D[23...0])

D[23...0] is illustrated for reference purposes below.

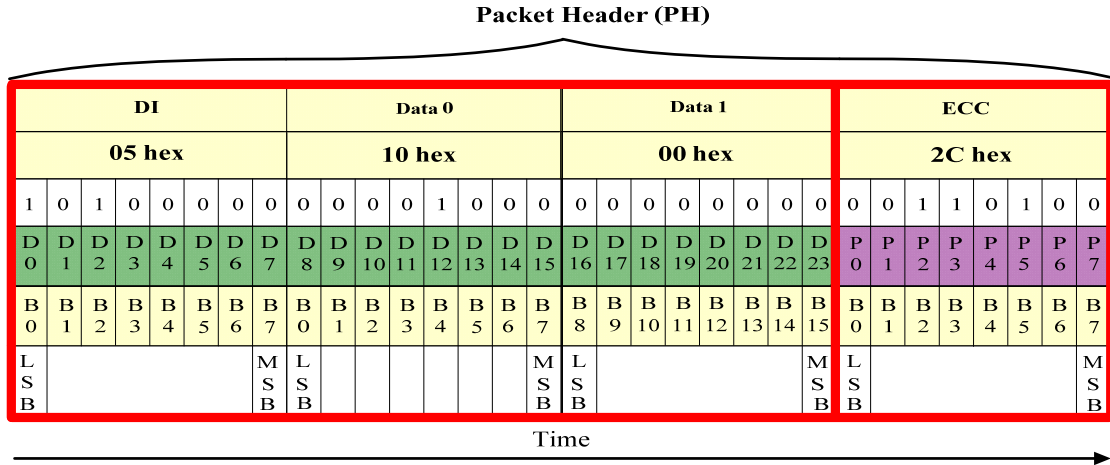


Figure: D[23:0] and P[7:0] on the short packet

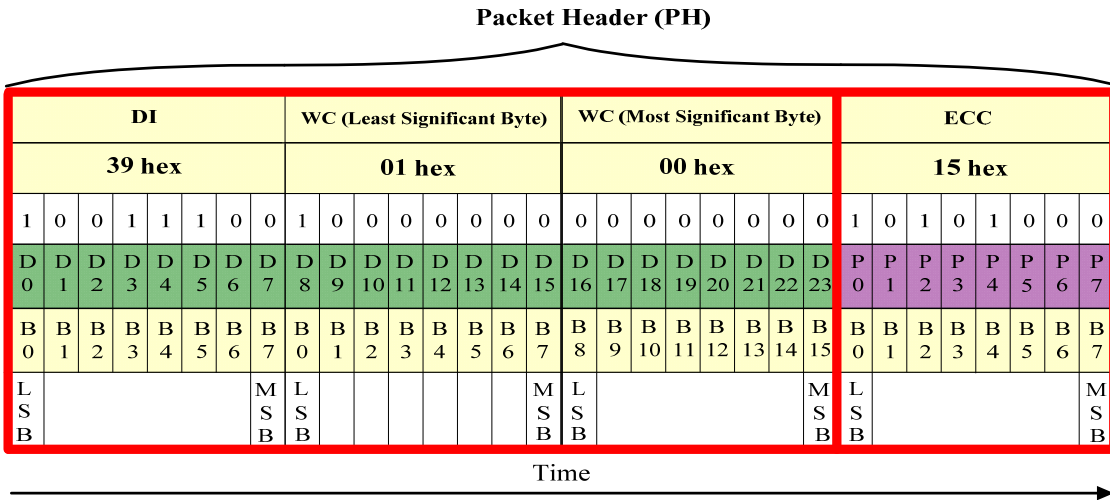


Figure: D[23:0] and P[7:0] on the long packet

Error Correction Code (ECC) can recognize one error or several errors and makes correction in one bit error case.

Bits (P[7...0]) of the Error Correction Code (ECC) are defined, where the symbol '^' is presenting XOR function (Pn is '1' if there is odd number of '1's and Pn is '0' if there is even number of '1's), as follows.

- P7 = 0
- P6 = 0
- P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23
- P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23
- P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23

- $P2 = D0 \wedge D2 \wedge D3 \wedge D5 \wedge D6 \wedge D9 \wedge D11 \wedge D12 \wedge D15 \wedge D18 \wedge D20 \wedge D21 \wedge D22$
- $P1 = D0 \wedge D1 \wedge D3 \wedge D4 \wedge D6 \wedge D8 \wedge D10 \wedge D12 \wedge D14 \wedge D17 \wedge D20 \wedge D21 \wedge D22 \wedge D23$
- $P0 = D0 \wedge D1 \wedge D2 \wedge D4 \wedge D5 \wedge D7 \wedge D10 \wedge D11 \wedge D13 \wedge D16 \wedge D20 \wedge D21 \wedge D22 \wedge D23$

P7 and P6 are set to '0' because Error Correction Code (ECC) is based on 64 bit value ([D63...0]), but this implementation is based on 24 bit value (D[23...0]). Therefore, there is only needed 6 bits (P[5...0]) for Error Correction Code (ECC).

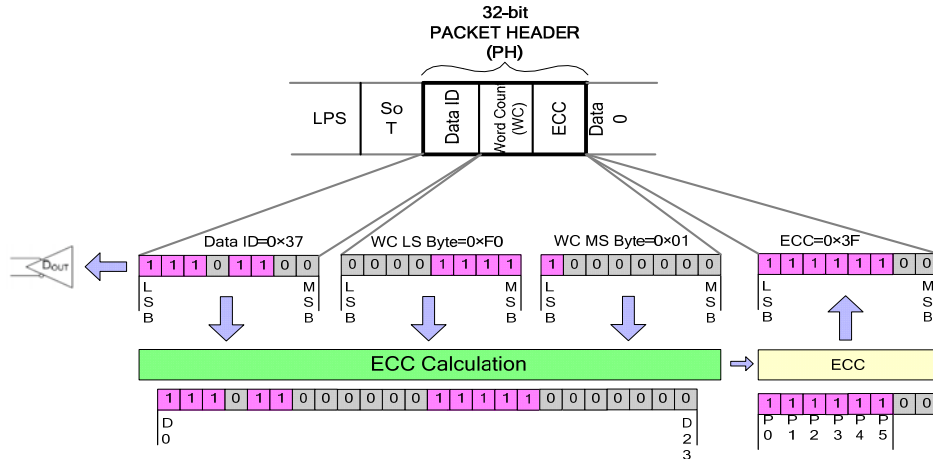


Figure: 24-bit ECC generation on TX side (Example)

### Packet footer on the long packet

Packet Footer (PF) of the Long Packet (Lpa) is defined after the Packet Data (PD) of the Long Packet (Lpa). The Packet Footer (PF) is a checksum value what is calculated from the Packet Data of the Long Packet (Lpa). The checksum is using a 16-bit Cyclic Redundancy Check (CRC) value which is generated with a polynomial  $X^{16}+X^{12}+X^5+X^0$  as it is illustrated below.

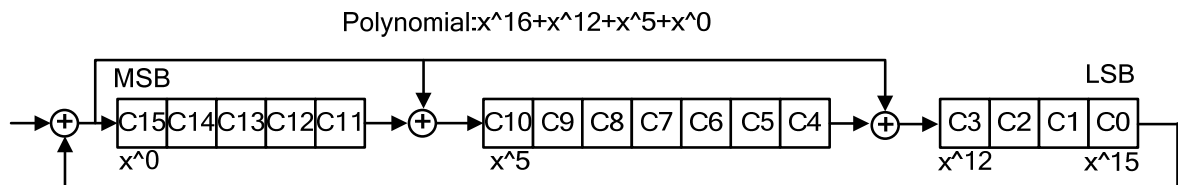


Figure: 16-bit cyclic redundancy check (CRC) calculation

The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations.

The Most Significant Bit (MSB) of the data byte of the Packet Data (PD) is the first bit what is inputted into the 16-bit Cyclic Redundancy Check (CRC).

The receiver is calculated own checksum value from received Packet Data (PD). The receiver compares own checksum and the Packet Footer (PF) what the transmitter has sent.

The received Packet Data (PD) and Packet Footer (PF) are correct if the own checksum of the receiver and Packet Footer (PF) are equal and vice versa the received Packet Data (PD) and Packet Footer (PF) are not correct if the own checksum of the receiver and Packet Footer (PF) are not equal.



6.2.4.2. Packet transmissions

Packet from the MCU to the display module

Display Command Set (DCS), which is defined on chapter “Instructions” is used from the MCU to the display module.

This Display Command Set (DCS) is always defined on the Data 0 of the Packet Data (PD), which is included in Short Packet (Spa) and Long packet (Lpa) as these are illustrated below.

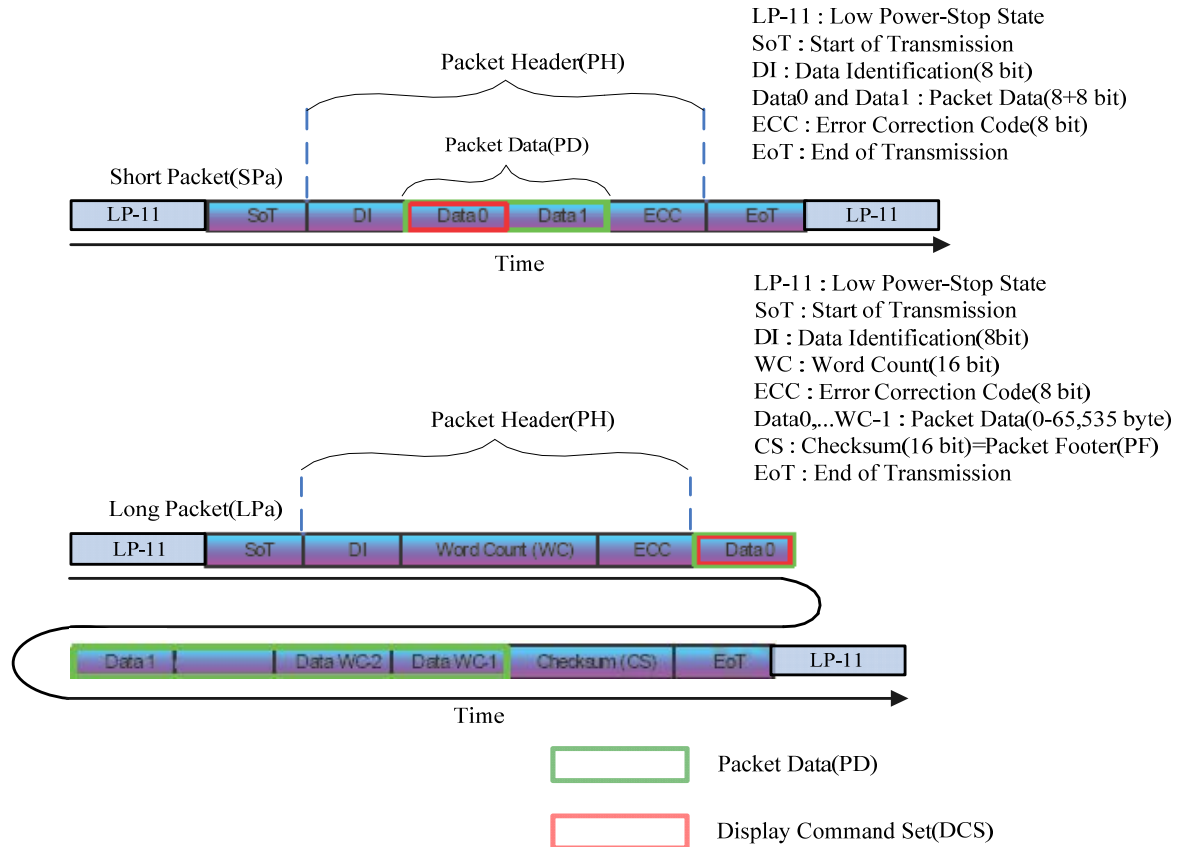


Figure: DCS on the short packet and long packet

Packet from the display module to the MCU

Used packet types

The display module is always using Short Packet (Spa) or Long Packet (Lpa), when it is returning information to the MCU after the MCU has requested information from the Display Module. This information can be a response of the Display Command Set (DCS).

The used packet type is defined on Data Type(DT).

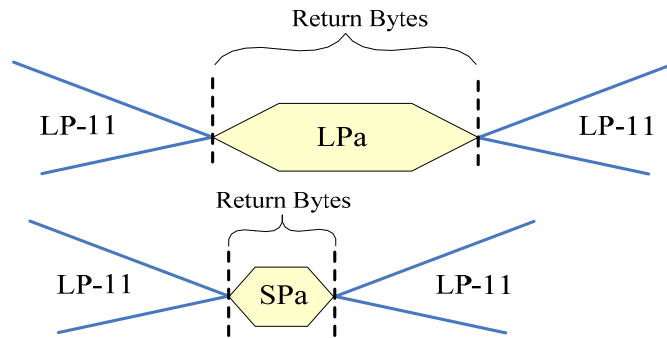


Figure: Return bytes on single packet

### Acknowledge with Error Report (AwER)

“Acknowledge with Error Report” (AwER) is always using a Short Packet (Spa), what is defined on Data Type (DT, 00 0010b), from the display module to the MCU.

The Packet Data (PD) can include bits, which are defining the current error, when a corresponding bit is set to 1, as they are defined on the following table.

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error,signal-bit(detected and corrected)
9	ECC Error,multi-bit(detected,not corrected)
10	Checksum(CRC)Error(only for Long Packet(LP))
11	DSI Data Type(DT)Not Recognized
12	DSI Virtual Channel(VC)ID Invalid
13	Invalid Transmission Length
14	Reserved,set to 0 internally
15	DSI Protocol violation

Table: Acknowledge with error report for long packet response

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error,signal-bit(detected and corrected)
9	ECC Error,multi-bit(detected,not corrected)
10	set to 0 internally
11	DSI Data Type(DT)Not Recognized
12	DSI Virtual Channel(VC)ID Invalid
13	Invalid Transmission Length
14	Reserved,set to 0 internally
15	DSI Protocol violation

Table: Acknowledge with error report for short packet response

These errors are only included on the last packet, which has been received from the MCU to the display module, before Bus Turnaround (BTA).

The display module ignores the received packet which includes error or errors.

Acknowledge with Error Report (AwER) of the Short Packet (Spa) is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7...6]): 00b
  - Data Type (DT, DI[5...0]): 00 0010b
- Packet Data (PD)
  - Bit 8: ECC Error, single-bit (detected and corrected)
  - AwER: 0100h
- Error Correction Code (ECC)

This is defined on the Short Packet (Spa) as follows.

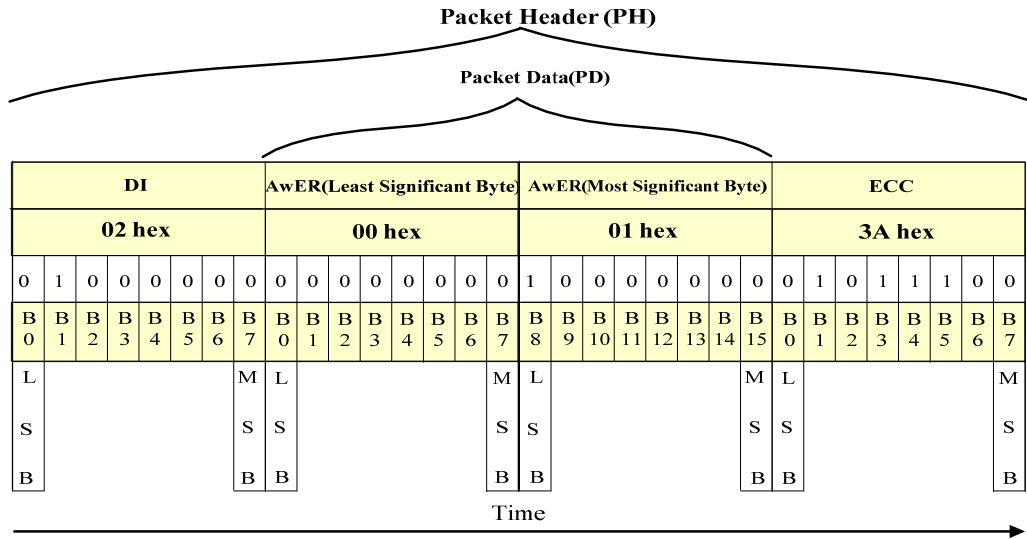
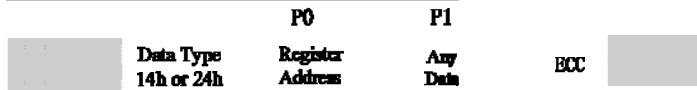


Figure: Acknowledge with error report – example

### 6.2.5. Customer-defined generic read data type format

NV3051F1 supports three types of generic read, generic read with no parameter, 1 parameter and 2 parameters. If NV3051F1 receives generic read with no parameter packet, it will return ack report. If NV3051F1 receives generic read with 1 parameter or 2 parameters packet, it will return generic short packet with 1 byte response.

#### Packet Structure (processor → peripheral)



#### Low Power Data Transfer (peripheral → processor)



Figure: Generic read data type format

**6.2.6. MIPI video parameter**

In the MIPI video mode, the frame is transmitted from the host processor to a display module as a sequence of pixels, with each horizontal line of the image data sent as a group of consecutive pixels.

Vsync (VS) indicates the beginning of each frame of the displayed image.

Hsync (HS) signals the beginning of each horizontal line of pixels.

Each pixel value (16-, 18-, or 24-bit data) is transferred from the host processor to the display module during one pixel period. The rising edge of PCLK is used by the display module to capture pixel data.

Since PCLK runs continuously, control signal DE is required to indicate when valid pixel data is being transmitted on the pixel data signals.

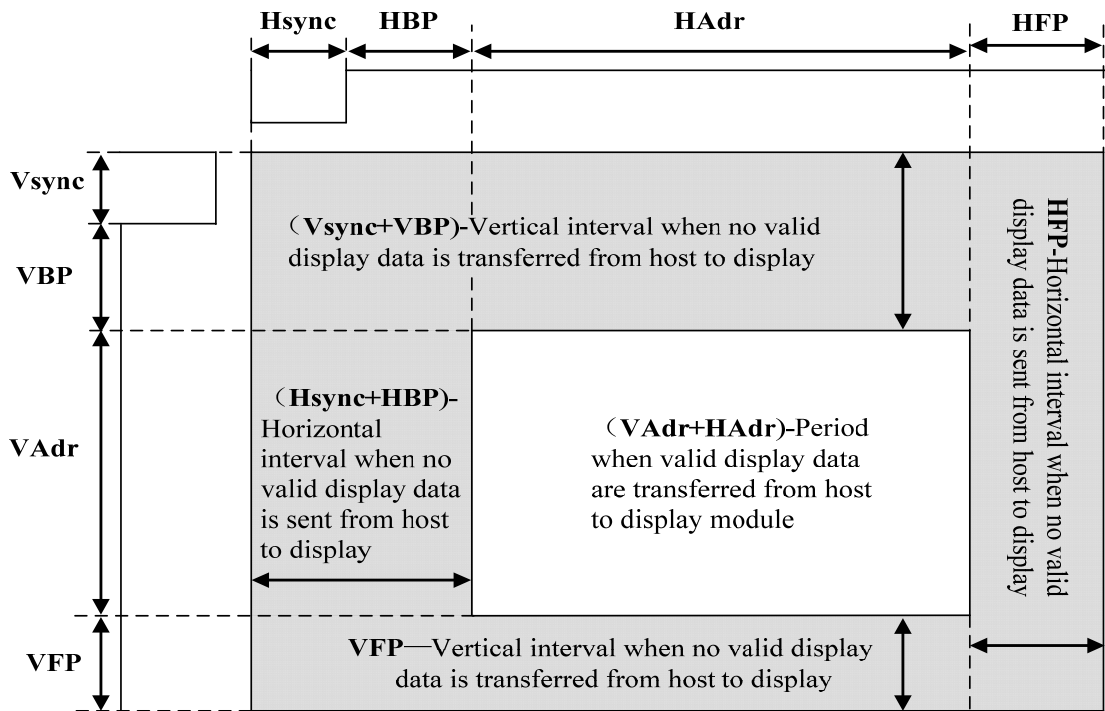


Figure define timing parameter for MIPI video operation

Below Table provide the timing parameter by external Vertical-cycle and Horizontal cycle and PCLK Frequency  
( Resolution for 800/720/640 horizontal x 1280 vertical display with Frame-Rate of 60Hz)

<b>Parameters</b>	<b>Symbols</b>	<b>Min.</b>	<b>Typ</b>	<b>Max.</b>	<b>Unit</b>
MIPI Vedio data-rate (4 lane)	-	-	500	-	Mbps
PCLK Frequency	FPCLK	TBD	63.92	-	MHz
Horizontal Synchronization	Hsync	TBD	2	-	PCLK
Horizontal Back Porch	HBP	TBD	44	-	PCLK
Horizontal Front Porch	HFP	TBD	46	-	PCLK
Hsync+ HBP+ HFP	-	TBD	90	-	PCLK
Horizontal Address (Display area)	Hadr	-	720	-	PCLK
Horizontal cycle	-	TBD	812	-	PCLK
Vertical Synchronization	Vsync	TBD	2	-	Line
Vertical Back Porch	VBP	TBD	14	-	Line
Vertical Front Porch	VFP	TBD	16	-	Line
Vsync+ VBP+ VFP	-	TBD	32	-	Line
Vertical Address (Display area)	Vadr	-	1280	-	Line
Vertical cycle	-	-	1312	-	Line
Frame-Rate			60		Hz

“-” means no limit.

Note1 : If using Image Process Algorithm, Typ value for H-blanking is minimum requirement.

Below Table provide the timing parameter by external Vertical-cycle and Horizontal cycle  
 (Resolution for 800/720/640 horizontal x 1280 vertical display with Frame-Rate of 60Hz)

Parameters	Symbols	Min.	Typ	Max.	Unit
MIPI Vedio data-rate (4 lane)	-	-	500	-	Mbps
PCLK Frequency	FPCLK	-	63.92	-	MHz
Horizontal Synchronization	Hsync	-	2	-	PCLK
Horizontal Back Porch	HBP	-	44	-	PCLK
Horizontal Front Porch	HFP	-	46	-	PCLK
Hsync+ HBP+ HFP	-	-	90	-	PCLK
Horizontal Address (Display area)	Hadr	-	720	-	PCLK
Horizontal cycle	-	-	12.703	-	us
Vertical Synchronization	Vsync	-	2	-	Line
Vertical Back Porch	VBP	-	14	-	Line
Vertical Front Porch	VFP	-	16	-	Line
Vsync+ VBP+ VFP	-	-	32	-	Line
Vertical Address (Display area)	Vadr	-	1280	-	Line
Vertical cycle	-	-	1312	-	Line
Frame-Rate	-	-	60	-	Hz

“-” means no limit.

Note : 1. If using Image Process Algorithm, Type value for H-blanking is minimum requirement.

Below Table provide the timing parameter by external Vertical-cycle  
 (Resolution for 800/720/640 horizontal x 1280 vertical display with Frame-Rate of 60Hz)

<b>Parameters</b>	<b>Symbols</b>	<b>Min.</b>	<b>Typ</b>	<b>Max.</b>	<b>Unit</b>
MIPI Vedio data-rate (4 lane)	-	-	500	-	Mbps
PCLK Frequency	FPCLK	-	63.92	-	MHz
Horizontal Synchronization	Hsync	-	2	-	PCLK
Horizontal Back Porch	HBP	-	44	-	PCLK
Horizontal Front Porch	HFP	-	46	-	PCLK
Hsync+ HBP+ HFP	-	-	90	-	PCLK
Horizontal Address (Display area)	Hadr	-	720	-	PCLK
Horizontal cycle	-	-	12.703	-	us
Vertical Synchronization	Vsync	-	2	-	Line
Vertical Back Porch	VBP	-	14	-	Line
Vertical Front Porch	VFP	-	16	-	Line
Vsync+ VBP+ VFP	-	-	32	-	Line
Vertical Address (Display area)	Vadr	-	1280	-	Line
Vertical cycle	-	-	16.66	-	ms
Frame-Rate	-	-	60	-	Hz

“-” means no limit.

Note : 1. If using Image Process Algorithm, Type value for H-blanking is minimum requirement.



### 6.3. Serial Interface (SPI)

The serial interface is used to communication between the micro controller and the LCD driver chip. It contains CSX (chip select), SCL (serial clock), SDI (serial data input) and SDO (serial data output). Serial clock (SCL) is used for interface with MPU only, so it can be stopped when no communication is necessary. If the host places the SDI line into high-impedance state during the read intervals, then the SDI and SDO can be tied together.

#### 6.3.1. SPI write mode

The write mode of the interface means the micro controller writes commands and data to the NV3051F1. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDI data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. When CSX is high, SCL clock is ignored. During the high time of CSX the serial interface is initialized. At the falling edge of CSX, SCL can be high or low. SDI/SDO is sampled at the rising edge of SCL. R/W indicates, whether the byte is read command(R/W = '1') or write command (R/W = '0'). It is sampled when first rising SCL edge. If CSX stays low after the last bit of command/data byte, the serial interface expects the R/W bit of the next byte at the next rising edge of SCL.

#### Register Write: Singal Parameter

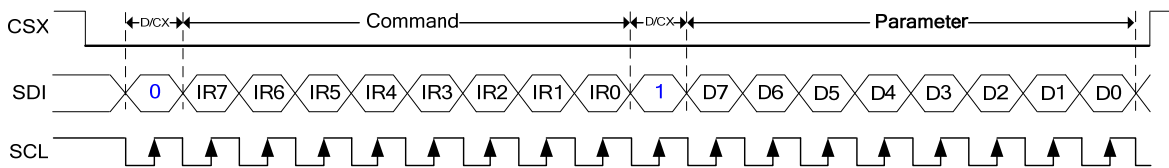


Figure: SPI Protocol for write

#### 6.3.2. SPI read mode

The read mode of the interface means that the micro controller reads register value from the NV3051F1. To do so the micro controller first has to send a command and then the following byte is transmitted in the opposite direction. After that CSX is required to go high before a new command is send. The NV3051F1 samples the SDI (input data) at the rising edges, but shifts SDO (output data) at the falling SCL edges.

Thus the micro controller is supported to read data at the rising SCL edges. After the read status command has been sent, the SDI line must be set to tri-state no later than at the falling SCL edge of the last bit. For the memory data read, a dummy clock cycle is needed (8 SCL clocks) to wait the memory data send out in SPI interface. But it doesn't need any dummy clock when execute the command data read.

#### Register Read: Without dummy clock

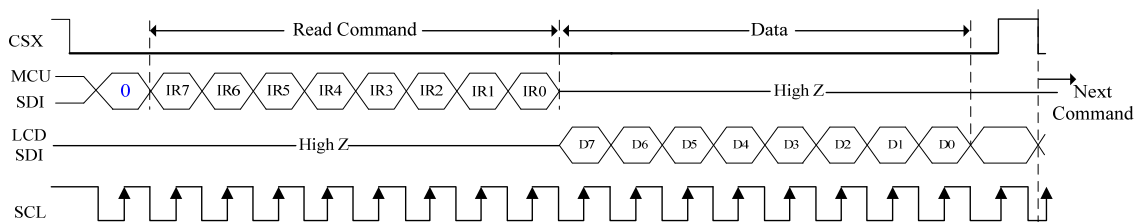
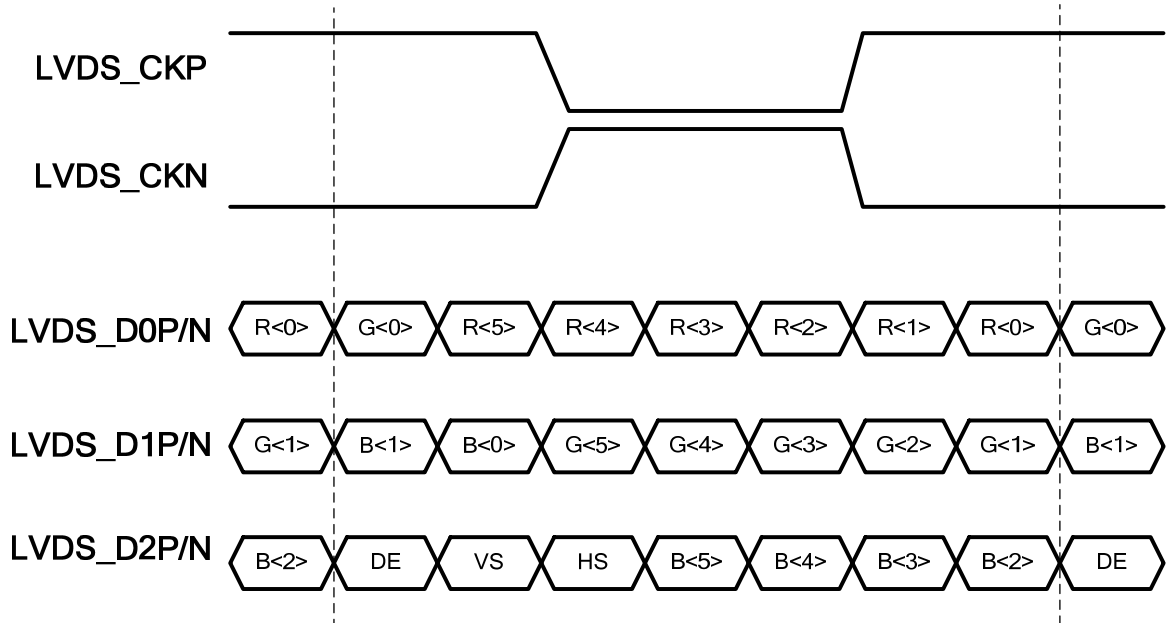


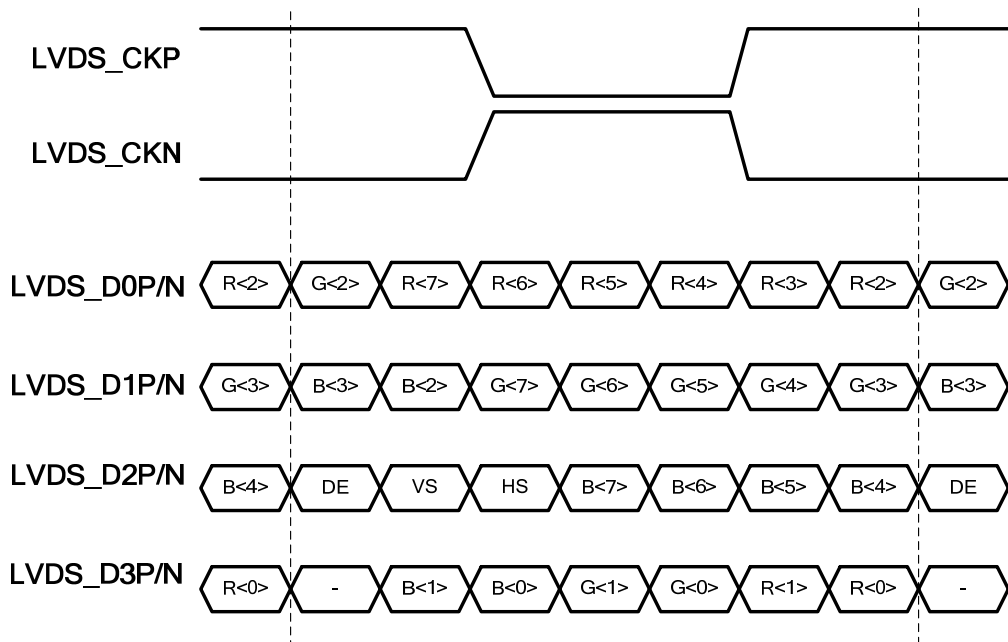
Figure: SPI Protocol for register read mode

## 6.4. LVDS interface

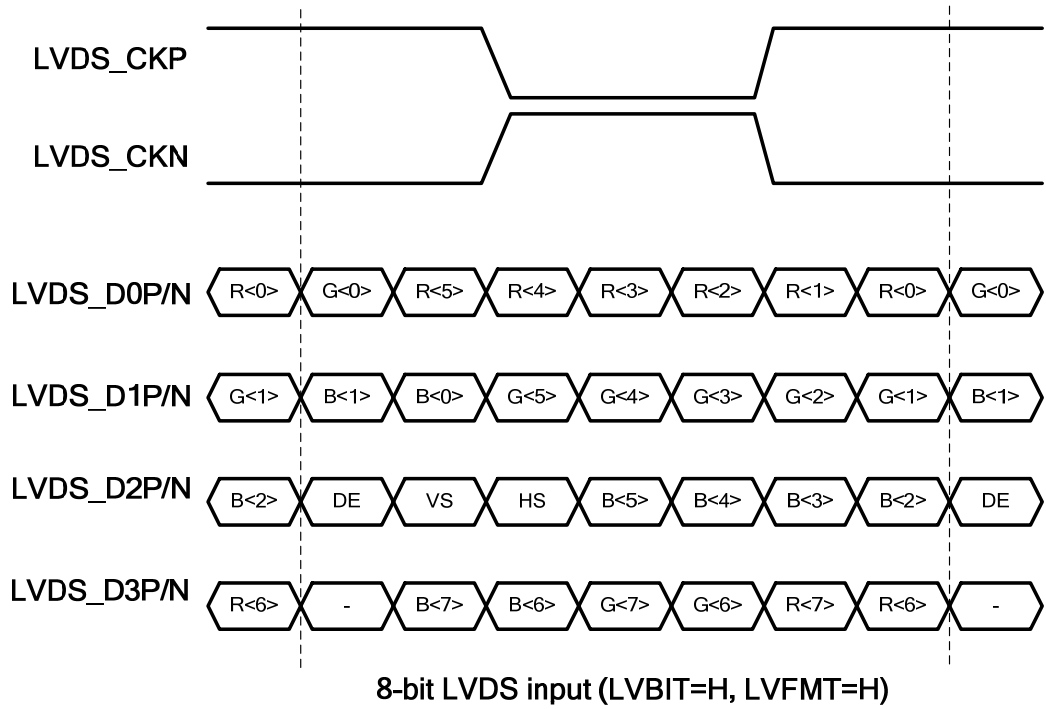
### 6.4.1 Data input format for LVDS



6-bit LVDS input (LVBIT=L, LVFMT=Don't care)



8-bit LVDS input (LVBIT=H, LVFMT=L)



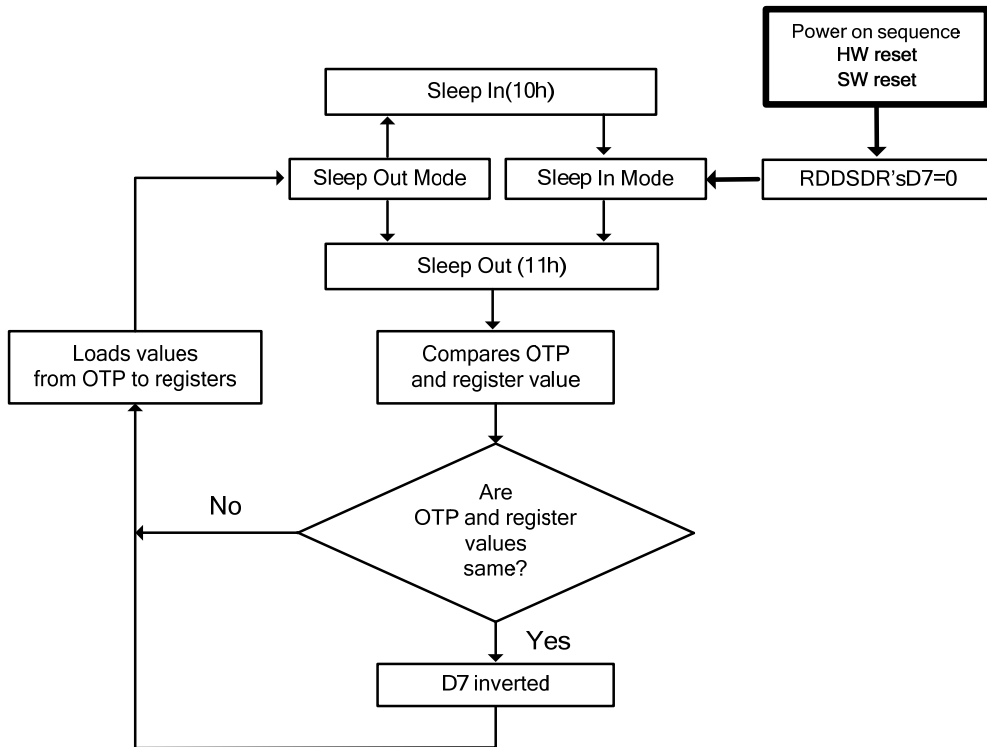
## 6.5. Sleep Out-Command And Self-Diagnostic Functions Of The Display Module

### 6.5.1. Register loading detection

Sleep Out-command is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from OTP (one-time programming memory) to registers of the display controller is working properly.

There are compared factory values of the OTP and register values of the display controller by the display controller. If those both values (OTP and register values) are same, there is inverted (=increased by 1) a bit in “Read Display Self-Diagnostic Result (0Fh)” (=RDDSDR) (The used bit of this command is D7). If those both values are not same, this bit (D7) is not inverted (= increased by 1).

The flow chart for this internal function is following:

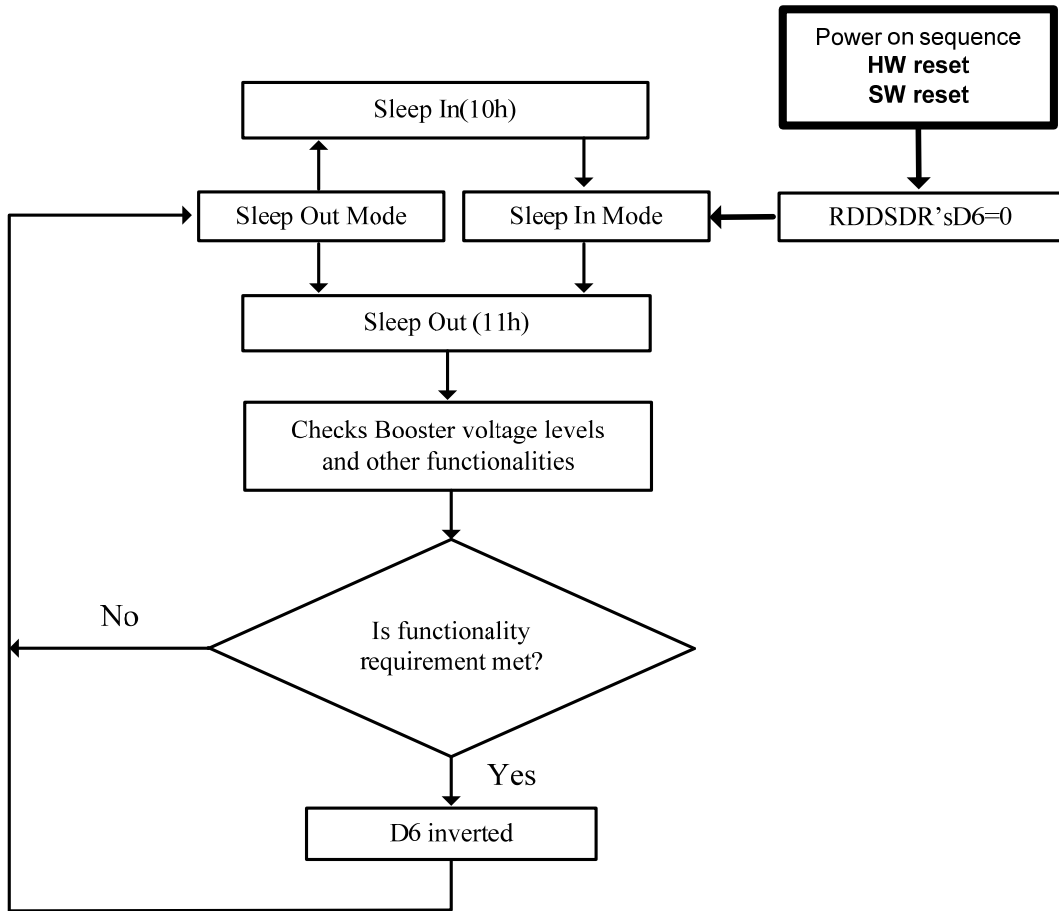


**6.5.2. Functionality detection**

Sleep Out-command is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (only Booster voltage level). If functionality requirement is met, there is inverted (= increased by 1) a bit in “Read Display Self-Diagnostic Result (0Fh)” (=RDDSDR) (The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (= increased by 1).

The flow chart for this internal function is following:



Note: There is needed 120msec after Sleep Out –command, when there is changing from Sleep In –mode to Sleep Out –mode, before there is possible to check if functionality requirements are met and a value of RDDSDR’s D6 is valid. Otherwise, there is 5msec delay for D6’s value, when Sleep Out –command is sent in Sleep Out –mode.

## **6.6. Power On/Off Sequence**

IOVCC and VCI can be applied in any order. IOVCC and VCI can be powered down in any order.

During power off, if LCD is in the Sleep Out mode, VCI and IOVCC must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, IOVCC or VCI can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

Note 1: There will be no damage to the display module if the power sequences are not met.

Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command.

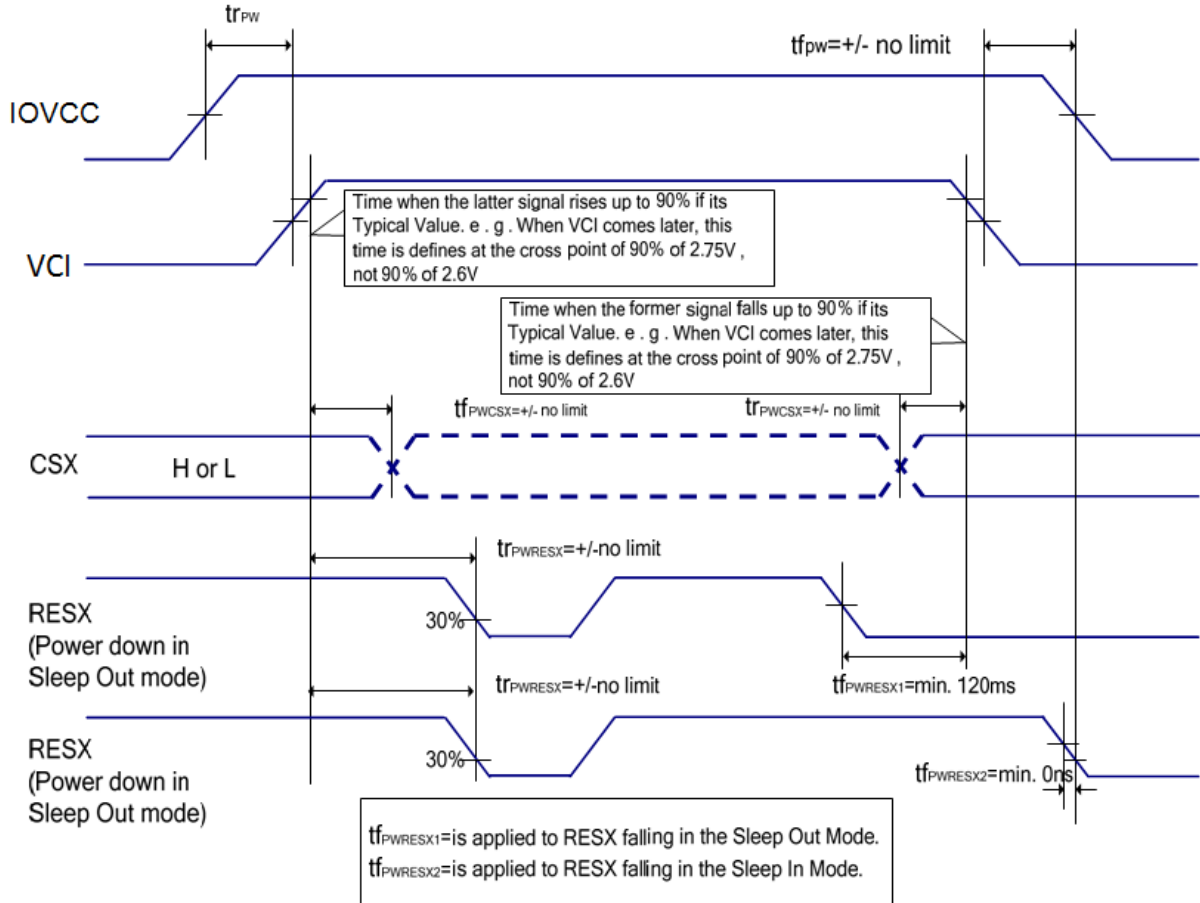
Also between receiving Sleep In command and Power Off Sequence.

If RESX line is not held stable by host during Power On Sequence, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below:

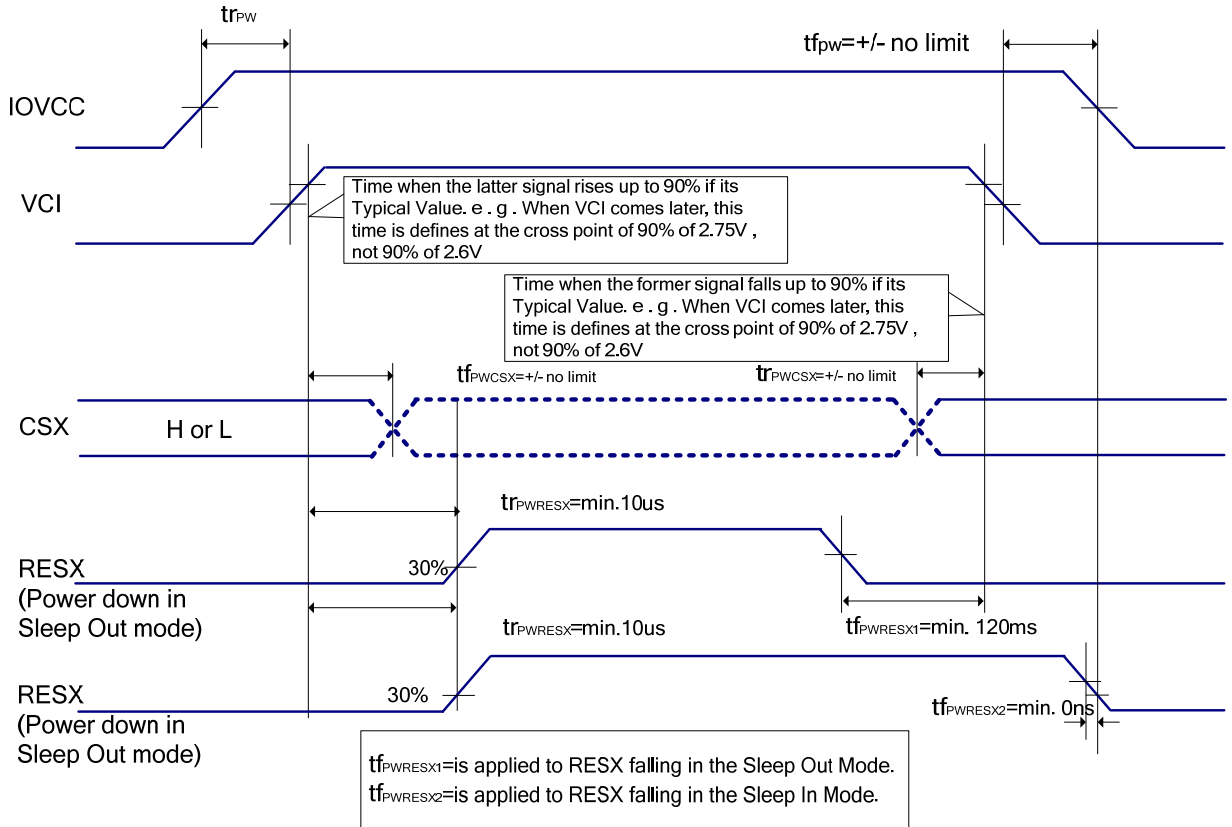
6.6.1. Case 1 – RESX line is held high or unstable by host at power on

If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and IOVCC have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



### 6.6.2. Case 2 – RESX line is held low or unstable by host at power on

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10sec after both VCI and IOVCC have been applied.



### 6.6.3. Uncontrolled power off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface.

At an uncontrolled power off the display will go blank and there will not be any visible effects within (TBD) second on the display (blank display) and remains blank until “Power On Sequence” powers it up.



## 7. ELECTRICAL SPECIFICATION

### 7.1. Absolute Maximum Ratings

(VCI=2.5V~6.0V, IOVCC = 1.65V~3.6V, Ta = -30°C ~ 70°C)

Parameter	Symbol	Rating	Unit	Note
Power Supply Voltage 1	IOVCC-VSS	-0.3 ~ +4.5	V	
Power Supply Voltage 2	VDDAM-VSS	-0.3 ~ +6.6	V	
Power Supply Voltage 3	VCI-VSS	-0.3 ~ +6.6	V	
Power Supply Voltage 4	VPP-VSS	-0.3 ~ +7.8	V	
Power Supply Voltage 5	DVDD-VSS	-0.3 ~ +1.8	V	
Power Supply Voltage 6	VSP-VSS	-0.3 ~ +6.6	V	
Power Supply Voltage 7	VSS-VSN	-0.3 ~ +6.6	V	
Power Supply Voltage 8	VGH-VGL	-0.3 ~ +32	V	
Input Voltage	Vt	-0.3 ~ IOVCC +0.3	V	
Operating Temperature	Topr	-30 ~ +70	°C	
Storage Temperature	Tstg	-40 ~ +85	°C	

Note: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

## 7.2. DC characteristic

### 7.2.1. Basic DC characteristic

(VCI=2.5V~6.0V, IOVCC = 1.65V~3.6V, Ta = -30°C ~ 70°C)

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
<b>Power &amp; Operation Voltage</b>							
Analog Operating voltage	VCI	Operating Voltage	2.5	2.8	6.0	V	
Logic Operating voltage	IOVCC	I/O supply voltage	1.65	1.8	3.6	V	
MIPI interface operating voltage	VDDAM	MIPI supply voltage	1.75	-	6.0	V	Note1
<b>Input/Output</b>							
Logic High level input voltage	VIH	-	0.7*IOVCC	-	IOVCC	V	
Logic Low level input voltage	VIL	-	VSS	-	0.3*IOVCC	V	
Logic High level output voltage	VOH	IOH = -0.1mA	0.8*IOVCC	-	IOVCC	V	
Logic Low level output voltage	VOL	IOL = +0.1mA	VSS	-	0.2*IOVCC	V	
Logic Input leakage current	IIL	Vin=IOVCC or VSSI	-0.1	-	+0.1	uA	
<b>VCOM Operation</b>							
VCOM voltage	VCOM	-	-3.375	-1.0	0	V	
<b>Source Driver</b>							
Source output range	Vsout	-	VGMIN+0.1	-	VGMP-0.1	V	
Gamma positive reference voltage	VGMP	-	2.62	-	5.68	V	
Gamma negative reference voltage	VGMIN	-	-5.68	-	-2.62	V	
Source output settling time	Tr	Below with 99% precision	-	TBD	-	us	
Output deviation voltage (Source positive output channel)	V <sub>dev</sub>	Sout >=+4.2V, Sout <=+0.8V	-	-	TBD	mV	
		+4.2V > Sout > +0.8V	-	-	TBD	mV	
Output deviation voltage (Source negative output channel)	V <sub>dev</sub>	Sout <=-4.2V, Sout >=-0.8V	-	-	TBD	mV	
		-4.2V < Sout < -0.8V	-	-	TBD	mV	

Output offset voltage	VOFFSET	-	-	-	TBD	mV	
<b>Reference Voltage</b>							
Internal reference voltage	VREF		1.876	2.00	2.125	V	
<b>Booster operation</b>							
1 <sup>st</sup> booster output voltage	VSP		4.5		6	V	
	VSN		-6		-4.5	V	
2 <sup>nd</sup> booster output voltage	VGH		11.0		18.0	V	
	VGL		-15.5		-7.0	V	
<b>Current Consumption</b>							
Sleep-IN mode	IIOVCC	RESX=High		TBD	TBD	uA	Note2
	IVCI			TBD	TBD	uA	
Deep standby mode	IIOVCC	RESX=High		TBD	TBD	uA	
	IVCI			TBD	TBD	uA	

Note1. VDDAM are used as the power of MVDD LDO, the voltage level can't be lower than 1.75V

Note2. The power/temperature conditions for Current consumption (Sleep-IN) part is (VCI, VDDAM) =3.0V, IOVCC=1.8V@25°C

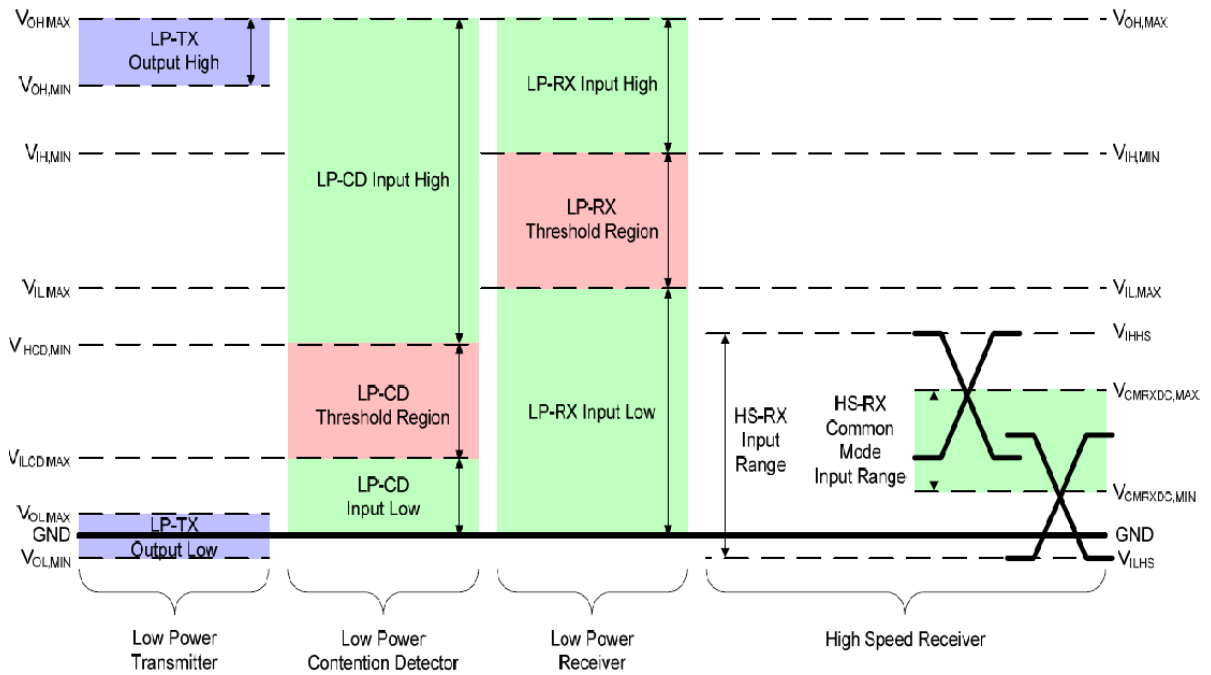
(These values might be updated after further evaluation.)

**7.2.2. MIPI DC character**

DC characteristics for MIPI-DSI

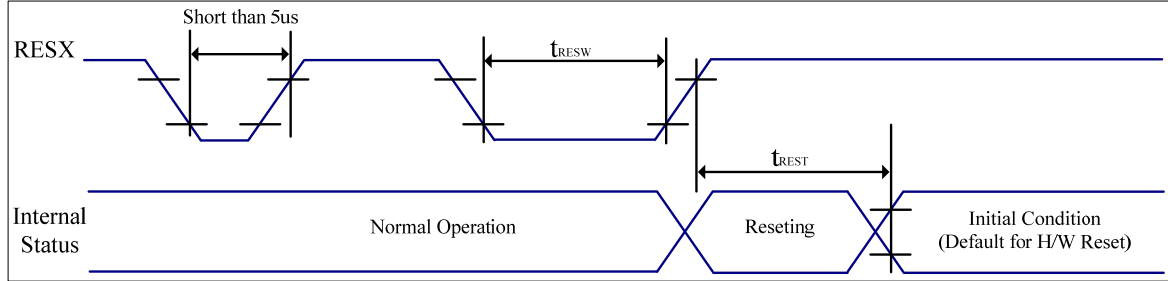
(VCI=2.5V~6.0V, IOVCC = 1.65V~3.6V, Ta = -30°C~70°C)

Parameter	Symbol	Conditions	Specification			Unit
			MIN	TYP	MAX	
<b>Power supply voltage for MIPI Interface</b>						
Power supply voltage for MIPI interface	VDDAM	-	1.75	1.8	6.0	V
	MV1P2	-	1.125	1.2	1.3	V
<b>LPDT Input Characteristics</b>						
Pad signal voltage range	VI	-	-50	-	1350	mV
Ground Shift	VGND SH	-	-50	-	50	mV
Logic 0 input threshold	VIL	-	0	-	550	mV
Logic 1 input threshold	VIH	-	880	-	MV1P2	mV
Input hysteresis	VHYST	-	25	-	-	mV
<b>LPDT Output Characteristics</b>						
Output low level	VOL	-	-50	-	50	mV
Output high level	VOH	-	1.1	1.2	1.3	V
Logic 1 contention threshold	VILCD,MIN	-	450	-	MV1P2	mV
Logic 0 contention threshold	VIHCD,MAX	-	0	-	200	mV
Output impedance of LPDT	ZOLP	-	80	100	125	ohm
<b>Hi-speed Input/Output Characteristics</b>						
Single-end input low voltage	VILHS	-	-40	-	-	mV
Single-end input high voltage	VIHHS	-	-	-	460	mV
Common mode voltage	VCMRXDC	-	70	-	330	mV
Hi-speed transmit voltage	VOD	-	140	200	250	mV
Differential input impedance	ZID	-	80	100	125	ohm



### 7.3. AC characteristic

#### 7.3.1. Reset timing characteristics



VSS=0V, IOVCC=1.65V to 3.6V, VCI=2.5V to 6.0V, Ta = -30°C to 70°C

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
$T_{resw}$	*1) Reset low pulse width	RESX	10	-	-	-	us
$T_{rest}$	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-	-	-	120	When reset applied during Sleep out mode	ms

Table: Reset input timing

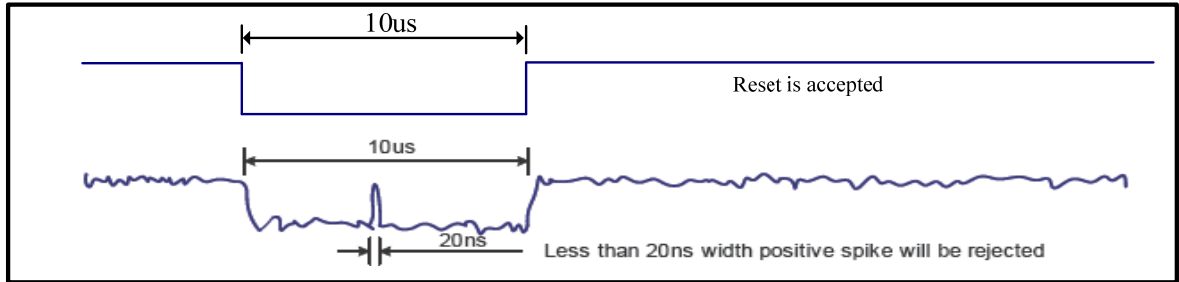
Note 1: Due to an electrostatic discharge on RESX line, spike does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts (It depends on voltage and temperature condition.)

Note 2: During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120ms, when Reset Starts in Sleep Out mode. The display remains the blank state in Sleep In mode), then return to default condition for H/W reset.

Note 3: During Reset Complete Time, ID1/ID2/ID3 and VCOM value in OTP will be latched to internal register. After a rising edge of RESX, there is a H/W reset complete time ( $T_{rest}$ ) which lasted 5ms. The loading operation will be done every time during this reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120 msec.

### 7.3.2. Serial interface characteristics (SPI)

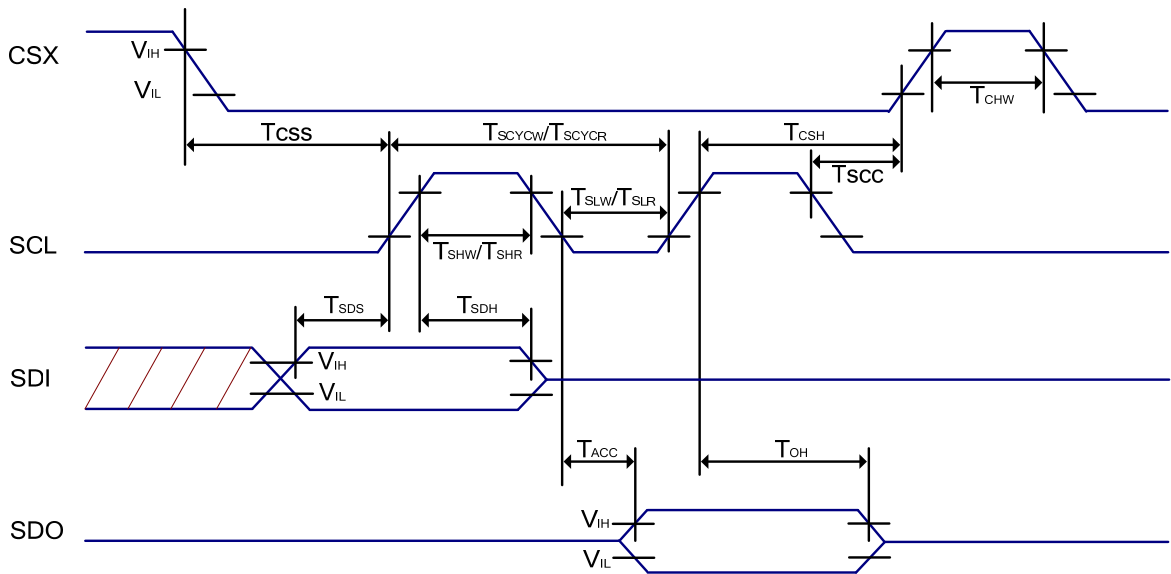


Figure: 3-pin Serial Interface Characteristics

Table: SPI Interface Characteristics

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T <sub>CSS</sub>	Chip select setup time	15	-	ns	-
	T <sub>CSH</sub>	Chip select hold time	15	-	ns	
	T <sub>SCC</sub>	Chip select setup time	20	-	ns	
	T <sub>CHW</sub>	Chip “H” pulse width	40	-	ns	
SCL	T <sub>SCYCW</sub>	Serial clock cycle (Write)	66	-	ns	-
	T <sub>SHW</sub>	SCL “H” pulse width (Write)	10	-	ns	
	T <sub>SLW</sub>	SCL “L” pulse width (Write)	10	-	ns	
	T <sub>SCYCR</sub>	Serial clock cycle (Read)	150	-	ns	-
	T <sub>SHR</sub>	SCL “H” pulse width (Read)	60	-	ns	
	T <sub>SLR</sub>	SCL “L” pulse width (Read)	60	-	ns	
SDI	T <sub>SDS</sub>	Data setup time	10	-	ns	-
	T <sub>SDH</sub>	Data hold time	10	-	ns	
	T <sub>ACC</sub>	Access time	10	50	ns	For maximum C <sub>L</sub> =30pf For minimum C <sub>L</sub> =8pf
	T <sub>OH</sub>	Output disable time	15	50	ns	

Note 1: IOVCC=1.65 to 3.6V, VCI=2.5 to 6V, VSSI=VSS=0V, Ta=-30 to 70°C

Note 2: The rise time and fall time (tr, tf) of input signal is specified at 15 ns or less.

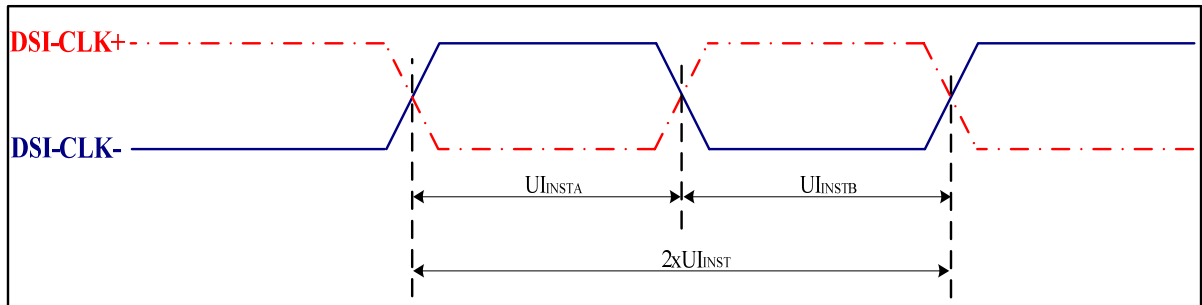
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.



7.3.3. MIPI-DSI characteristics

7.3.3.1. High speed mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
<b>High Speed Mode</b>						
DSI-CLK+/-	$2XU_{inst}$	Double UI instantaneous	2.22	-	25	ns
DSI-CLK+/-	$U_{INSTA}, U_{INSTB}$	UI instantaneous Halfs	1.11	-	12.5	ns
DSI-Dn+/-	$T_{ds}$	Data to clock setup time	0.15	-	-	UI
DSI-Dn+/-	$T_{dh}$	Data to clock hold time	0.15	-	-	UI
DSI-CLK+/-	$T_{drclk}$	Differential rise time for clock	150	-	0.3UI	ps
DSI-Dn+/-	$T_{drdata}$	Differential rise time for data	150	-	0.3UI	ps
DSI-CLK+/-	$T_{dfclk}$	Differential fall time for clock	150	-	0.3UI	ps
DSI-Dn+/-	$T_{dfdata}$	Differential fall time for data	150	-	0.3UI	ps



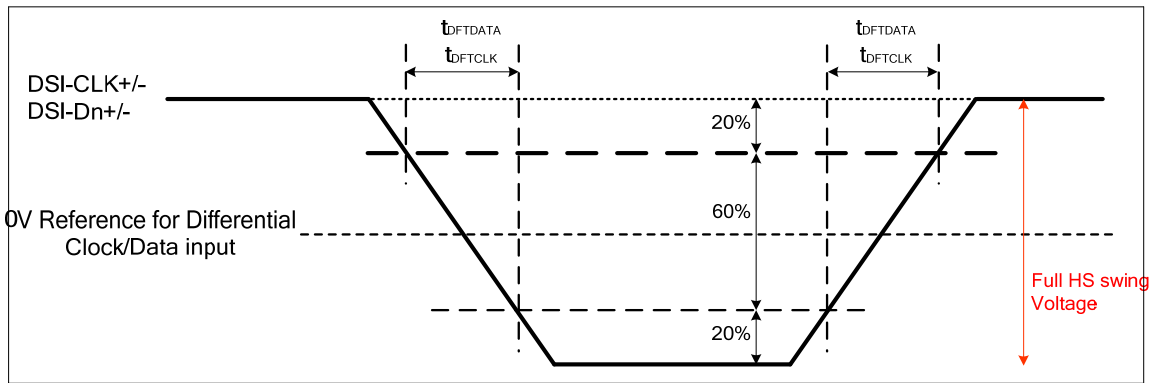
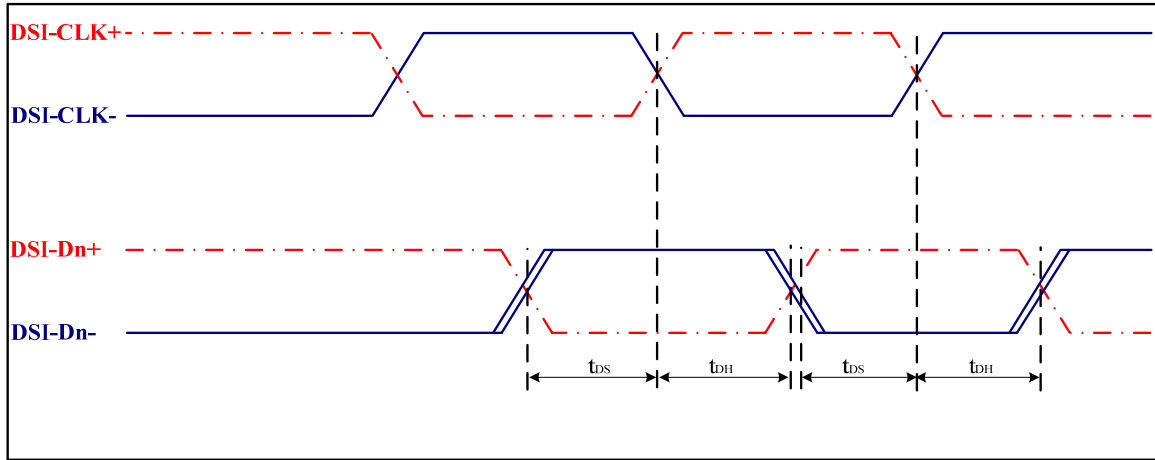


Figure: AC characteristics for MIPI-DSI High speed mode

7.3.3.2. Low power mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
<b>Low Power Mode</b>						
DSI-D0+/-	TLPXM	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU Display Module	50	-	-	ns
DSI- D0+/-	TLPXD	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Modulen MPU	58	-	-	ns
DSI- D0+/-	TTA-SURED	Time-out before the MPU start driving	TLPXD	-	2XTLPXD	ns
DSI- D0+/-	TTA-GETD	Time to drive LP-00 by display module	5XTLPXD	-	-	ns
DSI- D0+/-	TTA-GOD	Time to drive LP-00 after turnaround request – MPU	4XTLPXD	-	-	ns
DSI- D0+/-	Ratio TLPX	Ratio of TLPXM / TLPXD between MCU and display module	2/3	-	3/2	

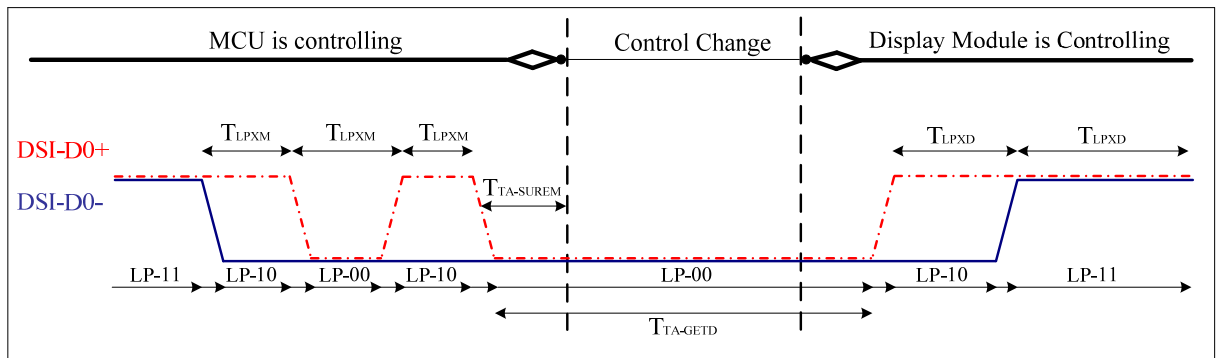


Figure: BTA from the MCU to the Display Module

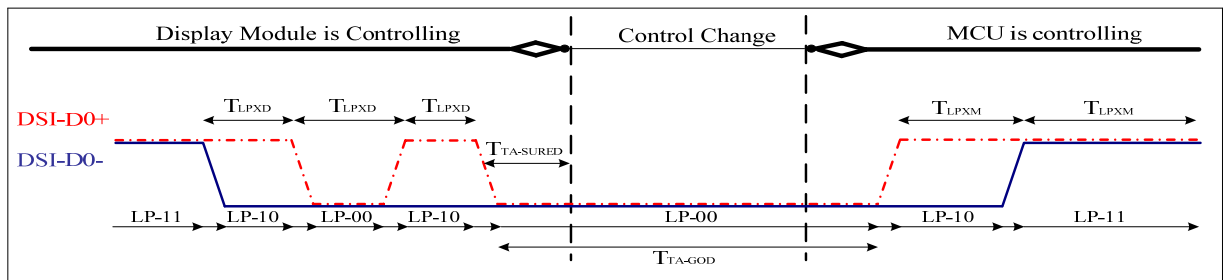


Figure: BTA from the Display Module to the MCU

7.3.3.3. Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
<b>High Speed Data Transmission Bursts</b>						
DSI-Dn+/-	TLPX	Length of any low-power state period	50	-	-	ns
DSI- Dn+/-	THS- PREPARE	Time to drive LP-00 to prepare for HS transmission	40ns+4UI	-	85ns+6UI	ns
DSI- Dn+/-	THS- PREPARE+THS- ZERO	THS-PREPARE+time to drive HS-0 before the sync sequence	145ns+10UI	-	-	ns
DSI- Dn+/-	TD-TERM- EN	Time to enable Data Lane receiver line termination measured from when Dn crosses VIL(max)	Time for Dn to reach VTERM-EN	-	35ns+4UI	ns
DSI- Dn+/-	THS-SKIP	Time-out at RX to ignore transition period of EoT	40	-	55ns+4UI	ns
DSI- Dn+/-	THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	max (8UI, 60ns+4UI)	-	-	ns
DSI- Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	-	ns
DSI- Dn+/-	TeoT	Time from start of THS-TRAIL period to start of LP-11 state	-	-	105ns+12UI	ns

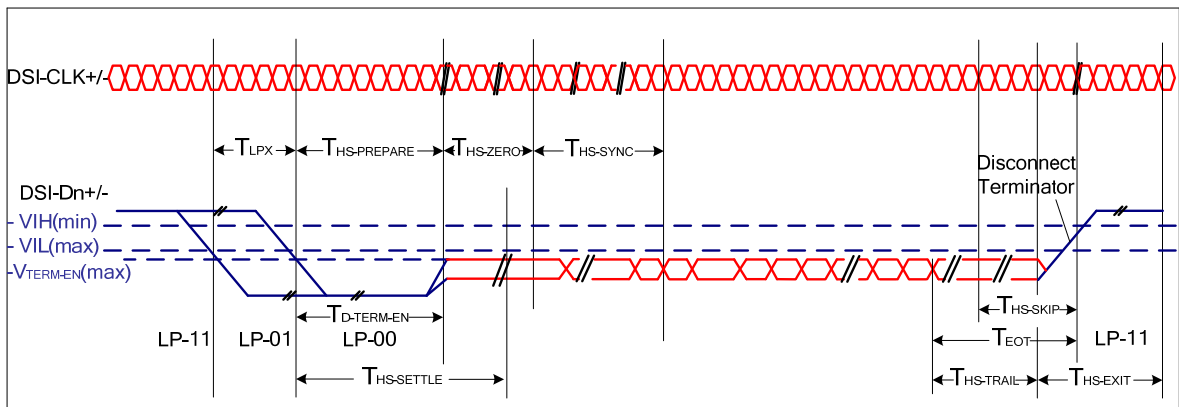


Figure: High Speed Data Transmission Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
<b>Switching the clock Lane between clock Transmission and Low Power Mode</b>						
DSI-CLK+/-	TCLK-POST	Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	60ns+52UI	-	-	ns
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8	-	-	UI
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS clock transmission	38	-	95	ns
DSI-CLK+/-	TCLK-TERM- EN	Time to enable Clock Lane receiver line termination measured from when Dn crosses $V_{IL(max)}$	Time for Dn to reach $V_{TERM-EN}$	-	38	ns
DSI- CLK+/-	TCLK-PREPARE +TCLK-ZERO	TCLK-PREPARE + time for lead HS-0 drive period before starting Clock	300	-	-	ns
DSI- CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns
DSI-CLK+/-	TeoT	Time from start of TCLK-TRAIL period to start of LP-11 state	-	-	105ns+ 12UI	ns

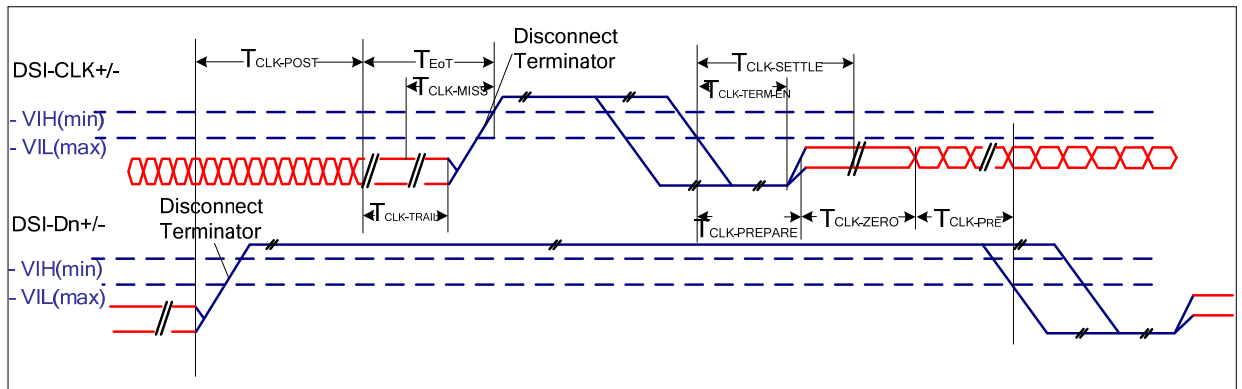


Figure: Switching the clock Lane between clock Transmission and Low Power Mode

7.3.4 LVDS AC characteristic

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock Frequency	RxFCLK	-	30	-	TBD	MHz
Input data skew margin	TRSKM	VID =200mV RxVCM=1.2V RxFCLK=81MHz	500	-	-	ps
Clock High Time	TLVCH	-	-	4/(7*RxFCLK)	-	ns
Clock Low Time	TLVCL	-	-	3/(7*RxFCLK)	-	ns
PLL wake-up-time	TenPLL	-	-	-	150	us

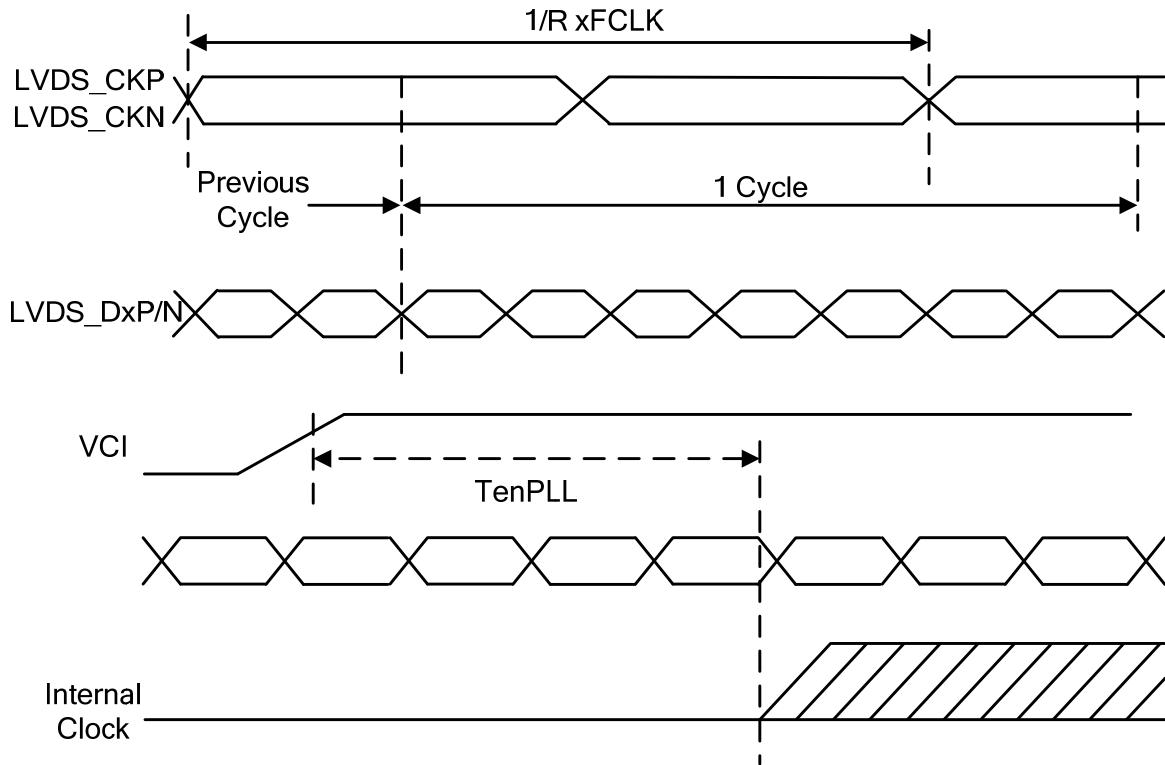
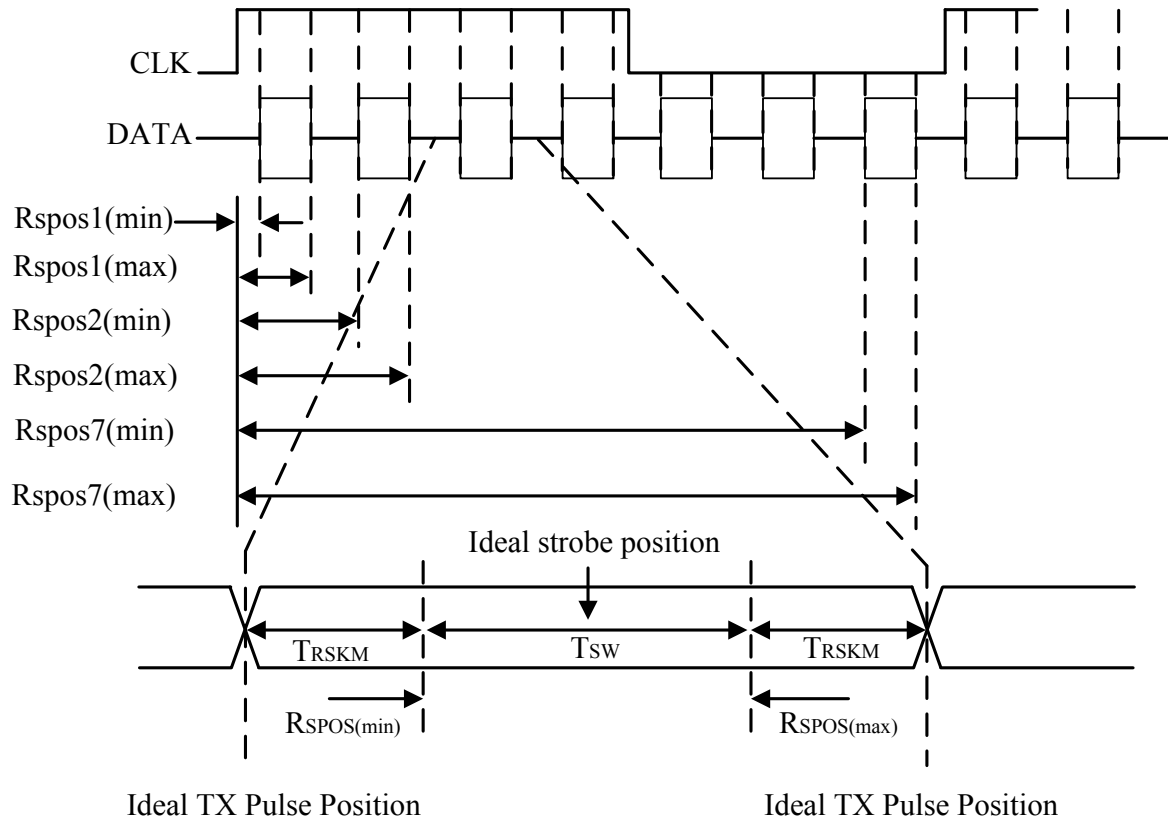


Figure LVDS figure

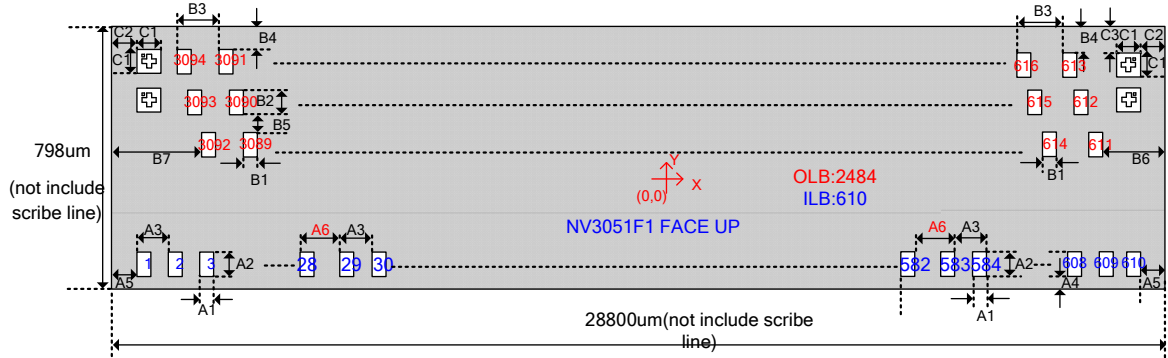
Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Modulation Frequency	SSCMF	23	-	93	KHz	
Modulation Rate	SSCMR	-	-	+3	%	



$T_{sw}$ : Strobe width (Internal data sampling window)  
 $RSPOS$ : Receiver strobe position  
 $T_{RSKM}$ : Receiver strobe margin

## 8. CHIP INFORMATION

### 8.1. PAD Assignment



Symbol	Size	Symbol	Size	Symbol	Size
A1	30	B1	16	B7	757.5
A2	48	B2	65	C1	60
A3	45	B3	33	C2	664
A4	13	B4	13	C3	10.9
A5	672.5	B5	25	Unit: um	
A6	55	B6	735.5		

Note: There is temperature compensation design.



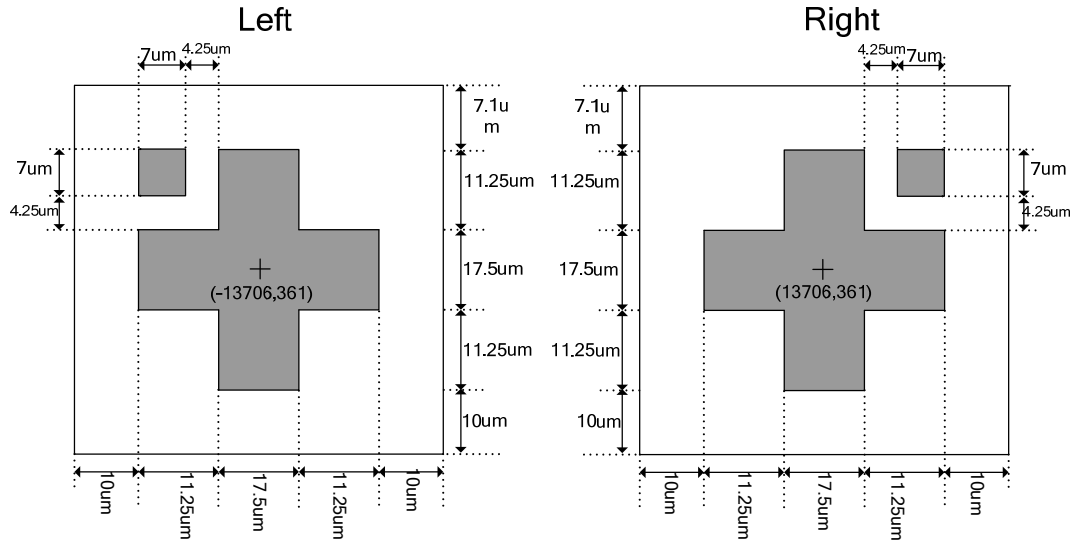
**Maximum layout resistance:**

Name	Type	Maximum layout resistance	Unit
IOVCC	Power supply	10	Ω
VDDAM	Power supply	10	Ω
VCI	Power supply	10	Ω
VSP,VSN	Power supply	10	Ω
DGND	Power supply	10	Ω
DGND_LVDS	Power supply	10	Ω
AGND	Power supply	10	Ω
VSSI	Power supply	10	Ω
VSSI_LVDS	Power supply	10	Ω
MGND	Power supply	10	Ω
CGND1	Power supply	10	Ω
RGND	Power supply	10	Ω
VPP	Power supply	10	Ω
IM[2:0],LANSEL	Input	100	Ω
EXTP,EXTN	Output	30	Ω
SCL,CSX,RESX	Input	100	Ω
SDI	Input/Output	100	Ω
SDO	Output	100	Ω
TE, TE1	Output	100	Ω
LEDPWM	Output	100	Ω
PWM_VSN	Output	100	Ω
CLKP;CLKN	Input	8	Ω
D0P/N~D3P/N	Input/Output	8	Ω
LVDS_CK;LVDS_CKN	Input	5	Ω
LVDS_D0P/N~LVDS_D3P/N	Input	5	Ω
DVDD	Output	10	Ω
DVDD_LVDS	Output	10	Ω
VGMP, VGMN	Output	10	Ω
VREF	Output	10	Ω
VGH	Output	10	Ω
VGL	Output	10	Ω
MVDD	Output	10	Ω
GOUT_L[22:1]	Output	30	Ω
GOUT_R[22:1]	Output	30	Ω
VCOM_L,VCOM_R,VCOM_DUM	Output	10	Ω
TEST_EN,BIST_EN,CLK_SEL	Input	100	Ω
EXT_CLK,TEST[3:0]	Input	30	Ω
TOUT[3:0]	Output	30	Ω
LED_K1; LED_K2; LED_k3; LED_k4; LED_k5	Input/Output	5	Ω
RS1	Input	100	Ω
VGH1,VGH2	Output/Capacitor Connection	10	Ω
DCHR1, DCHR2	Output/Resistor Connection	50	Ω

## 8.2. Alignment Mark

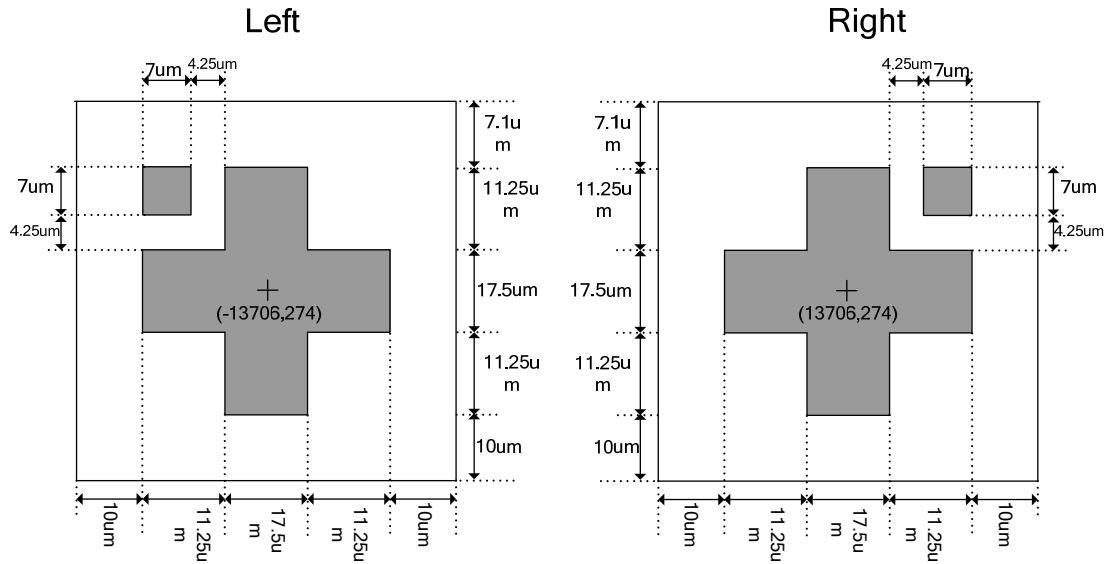
--Alignment Mark coordinate

Left1 (-13706,361),Right1 (13706,361)



Left2 (-13706, 274),Right2 (13706, 274)

--Alignment Mark size



## **9. DISCLAIMER**

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### Revision history

Version No.	Date	Page	Introduction
0.1	2020-11-19	All	New build.
0.2	2020-12-3	P4	Change“800xRGBx1280 pixels in resolution” to 800xRGBx2048 pixels in resolution.
0.3	2020-12-25	P5	Add“IGZO-LCD”.
		P6	Add“ Note: $3V \leq IOVCC \leq 3.6V$ for using LVDS”.

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